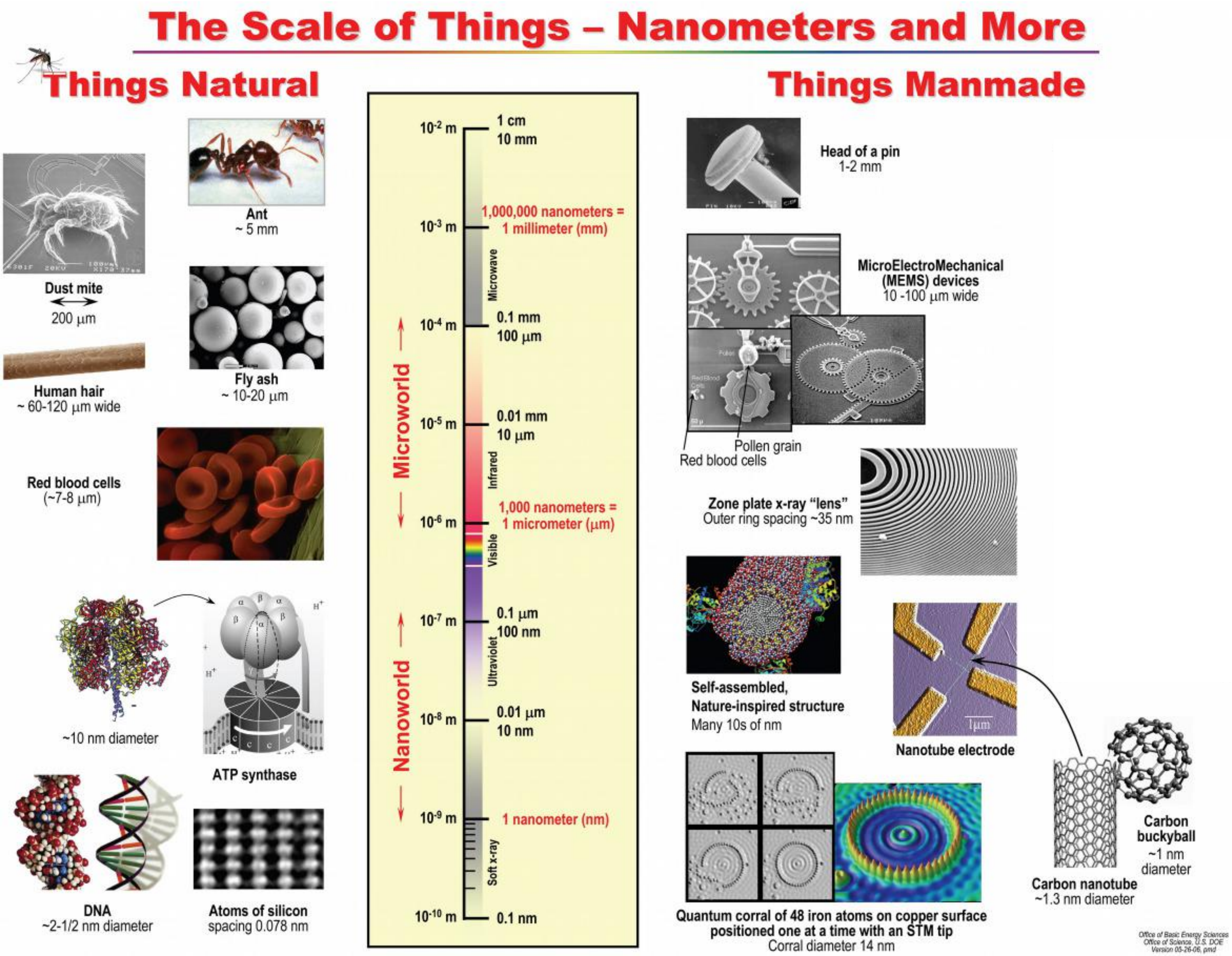
Micro & Nano Fabrication techniques

Dominique Mailly
Centre de Nanosciences et de Nanotechnologie
CNRS - Marcoussis

Ouline of the lecture

- Introduction to nanofabrication techniques and microelectronics
- Lithography techniques:
  - Optical lithography
  - Lithography using focused beams:
    - Electron beam lithography
    - Ion beam lithography
  - Near field techniques
  - Imprint techniques
- Metal and dielectric deposition techniques:
  - Thermal evaporation
  - Chemical vapor deposition
  - Atomic layer deposition
- Transfer techniques
  - Chemical wet etching
  - Ion beam etching
  - Reactive ion beam etching

Introduction:length scales



Micro and nanofabrication

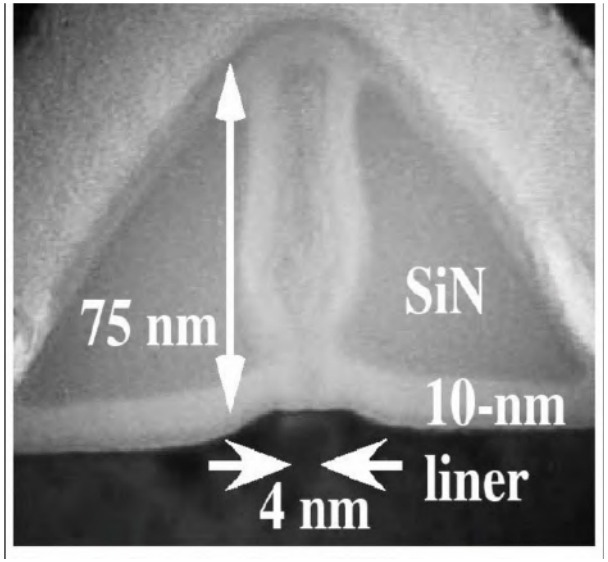
- Microfabrication is the process of fabricating structures from few decade of micrometer down to a tenth of micrometer
- Nanofabrication is the process of fabricating structures of size below 100nm.
- There is some debate to set how many space direction need to be taylored.
- Usually if only one direction is involved (2d- film) this is not really considers as nanofabrication (spill oil on water..)
- The microelectronics industry has continously pushed Micro & Nanofab performance since the 60’s

Historical review of microelectronics

- **1947 : first transistor (Bardeen, Brattain, Shockley, Nobel price 1956)**
- **1957: first use of photolithography**
- **1959: first integrated circuits (→ Nobel 2000 for Noyce and Kilby)**

http://www.nobel.se/physics/educational/transistor/function/index.html

The first transistor

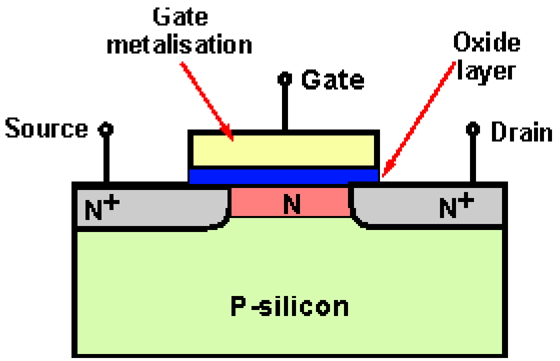


Today’s transistor

Nowdays the length of the gate of the smallest functional transistors are below 10nm

MOSFET

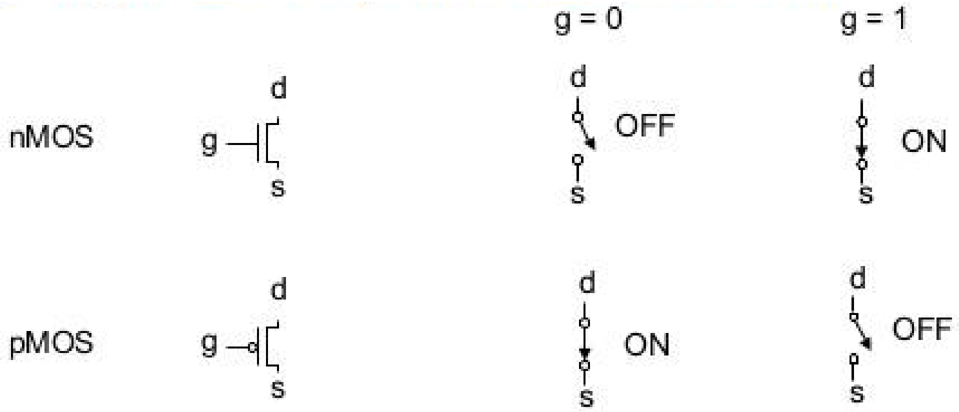
- **<u>Metal Oxyde semiconductor Field Effect Transistor (MOSFET)</u>**



Either:

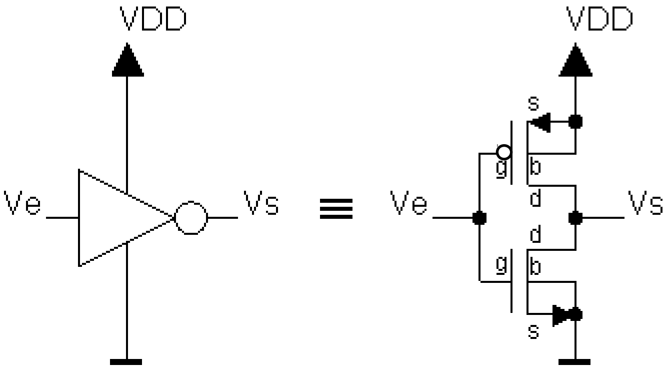
→voltage controled switch

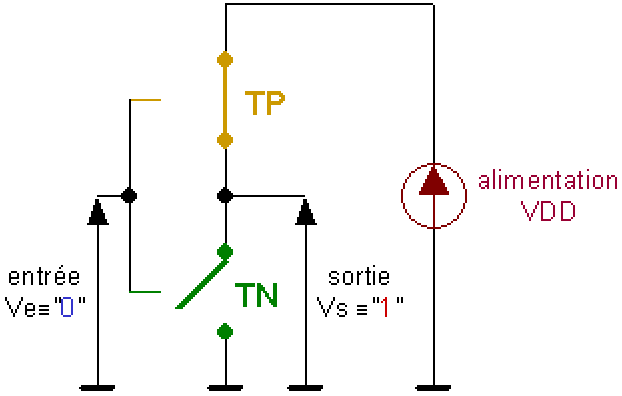
→signal amplifier

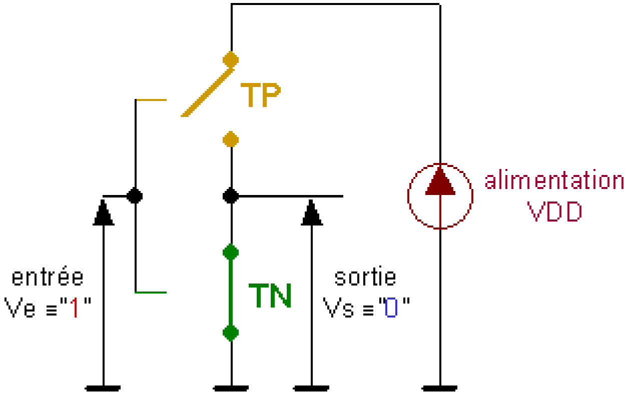


CMOS = complementary MOS

Association of a nMOS and a pMOS

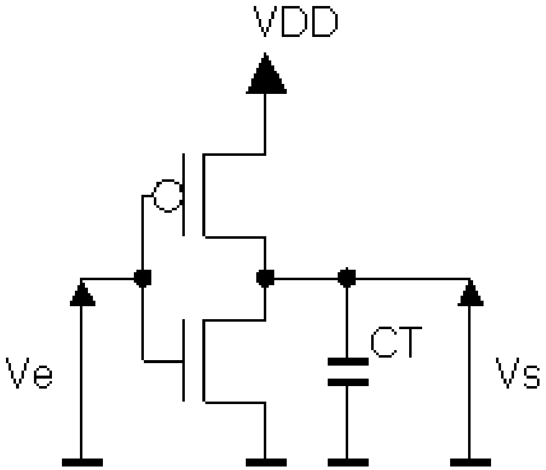






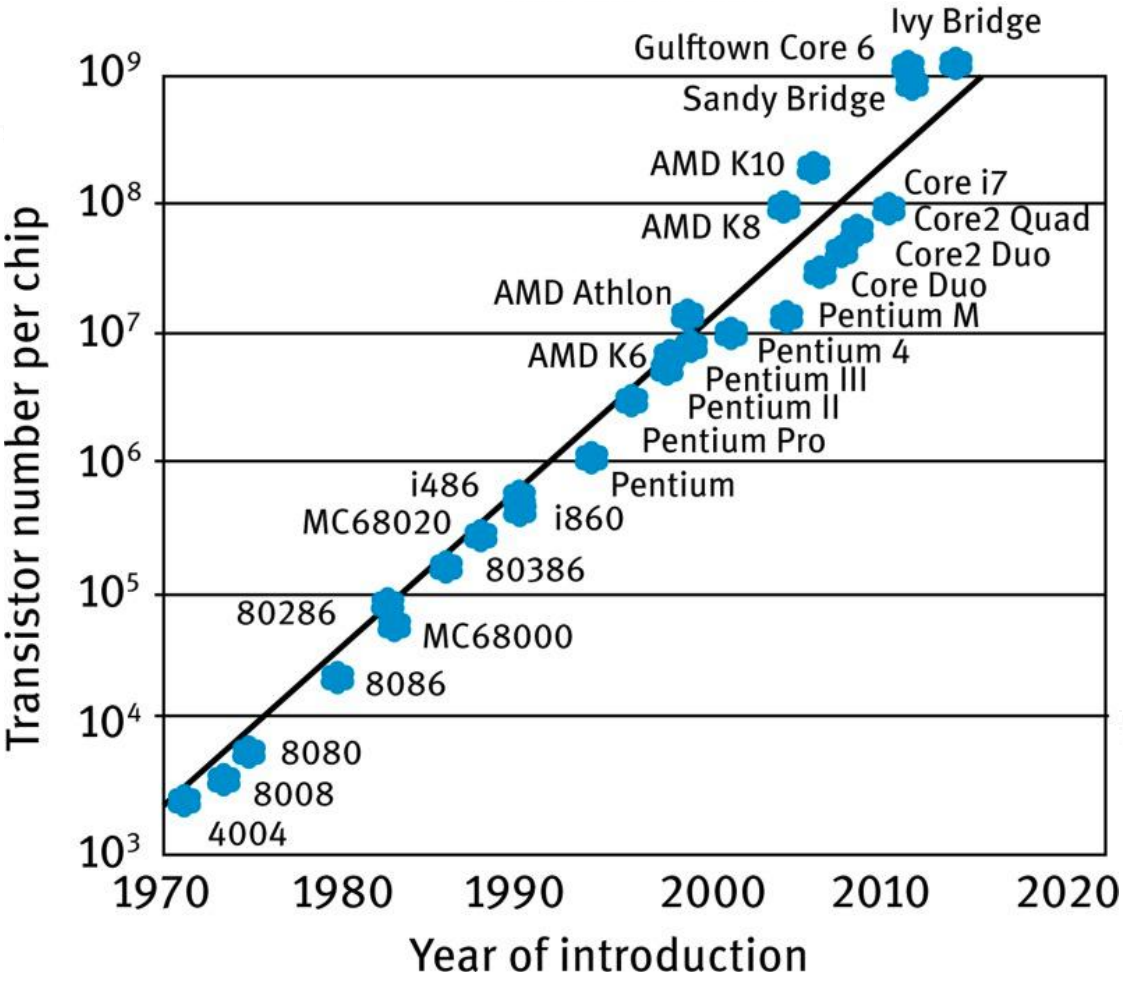
No current is flowing in the static regime

CMOS inverteur



- During the switch of Ve the source bring the energy needed to discharge the equivalent capacitor CT of the circuit.
- This abscence of dissipation in the static regime allowed the drastic increase of transistor in the IC’s since 1970.

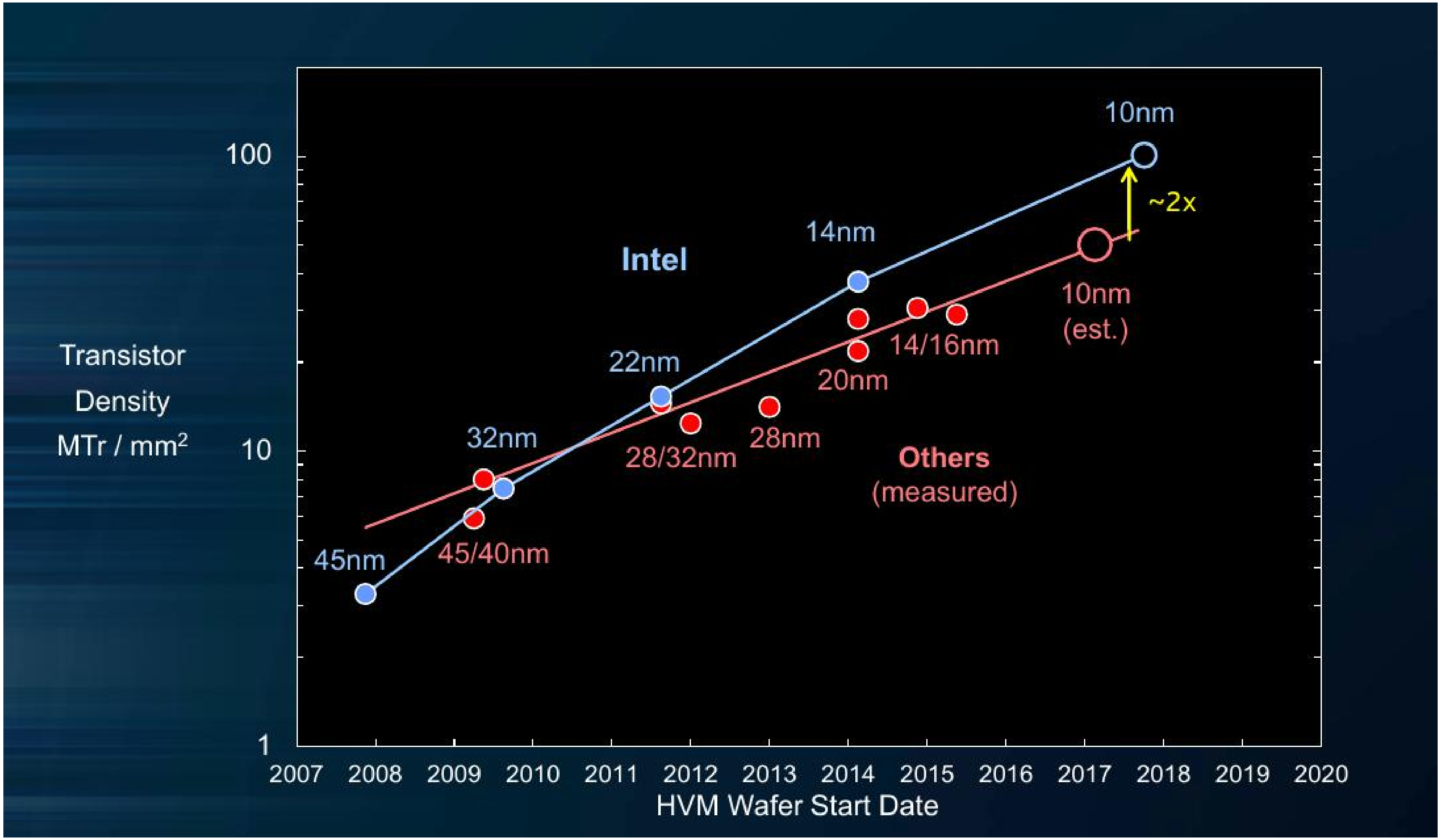
Transistor number per chip : the Moore's law



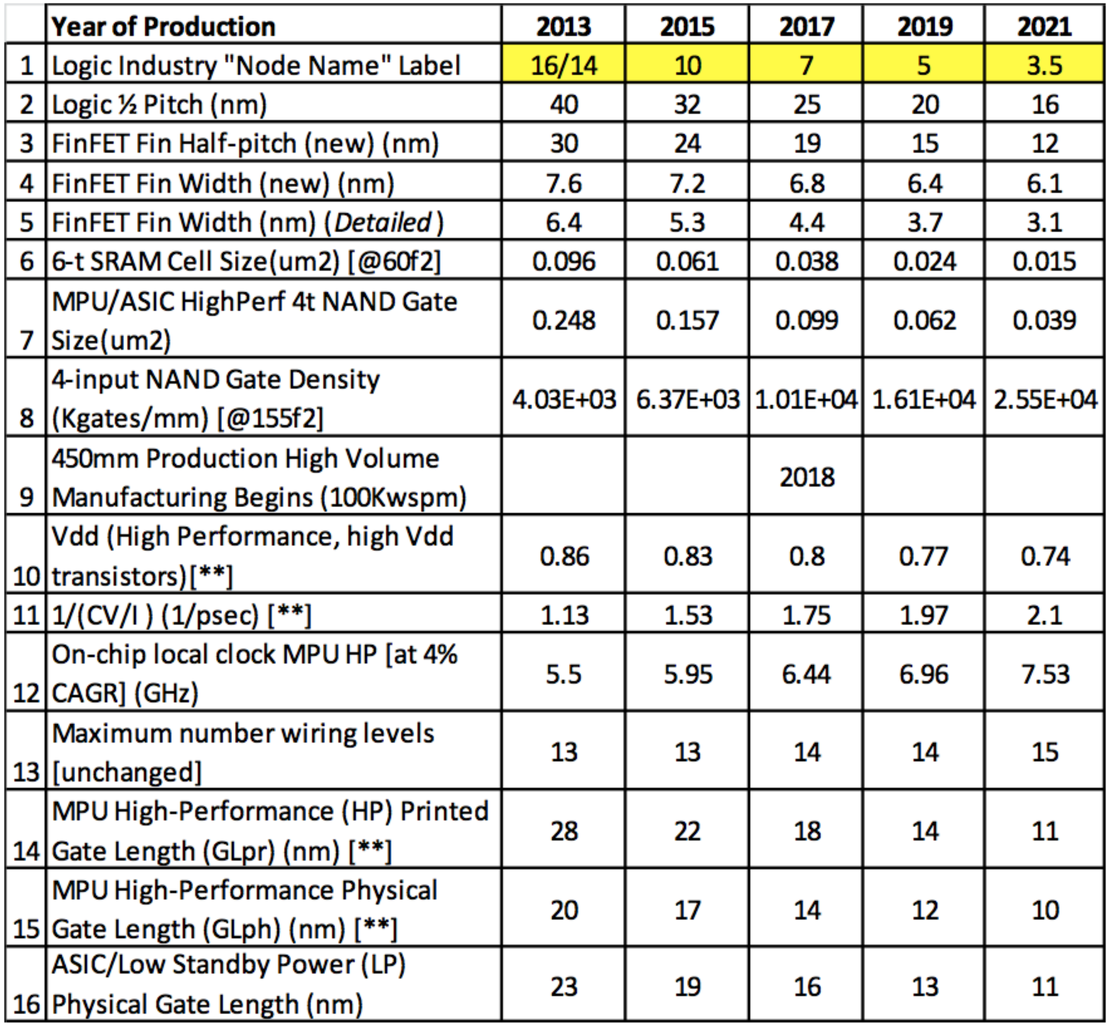
Gordon Moore

The number of transistor double every 18 months

Moore’s law

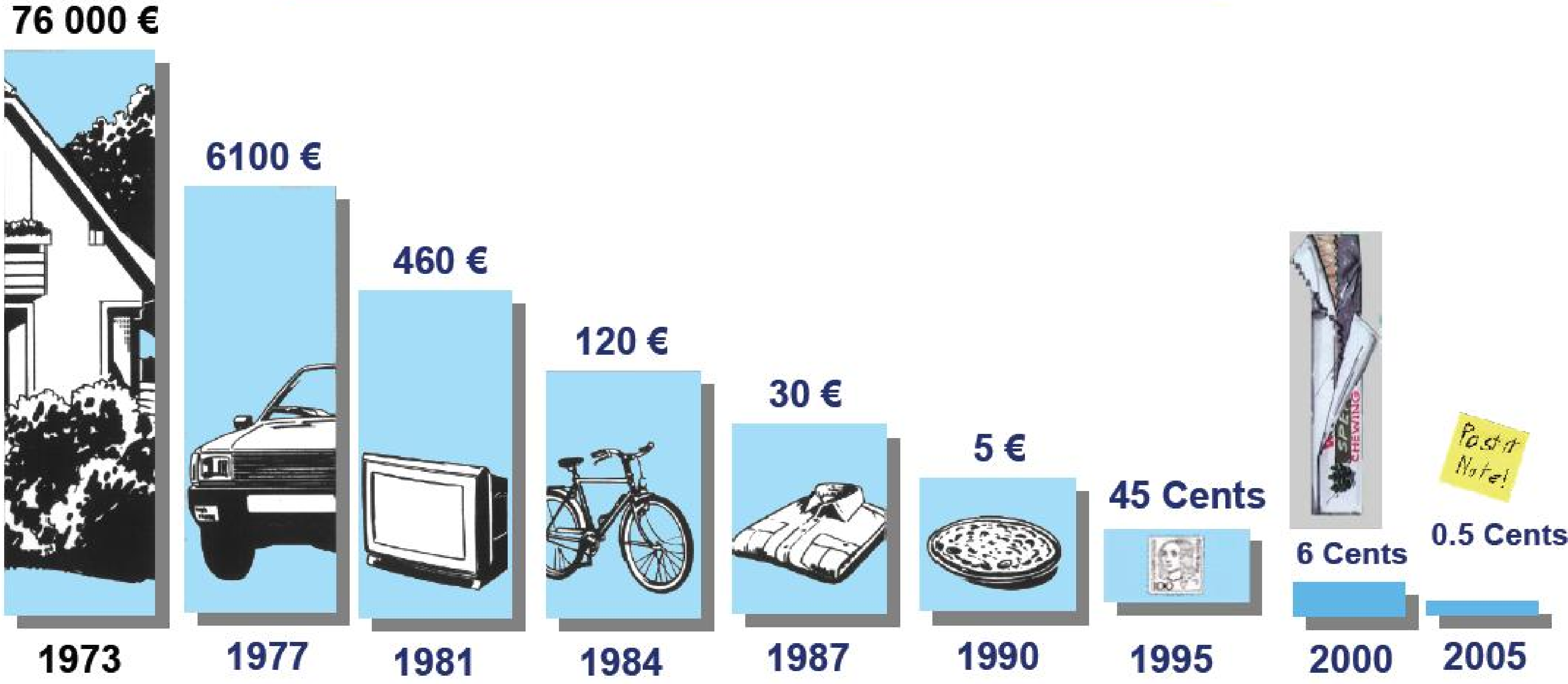

Transistor Density MTr / mm²
100
10
1
2007
2008
2009
2010
2011
2012
2013
2014
2015
2016
2017
2018
2019
2020
HVM Wafer Start Date
Intel
45nm
32nm
22nm
14nm
10nm
~2x
45/40nm
28/32nm
28nm
20nm
14/16nm
10nm (est.)
Others (measured)

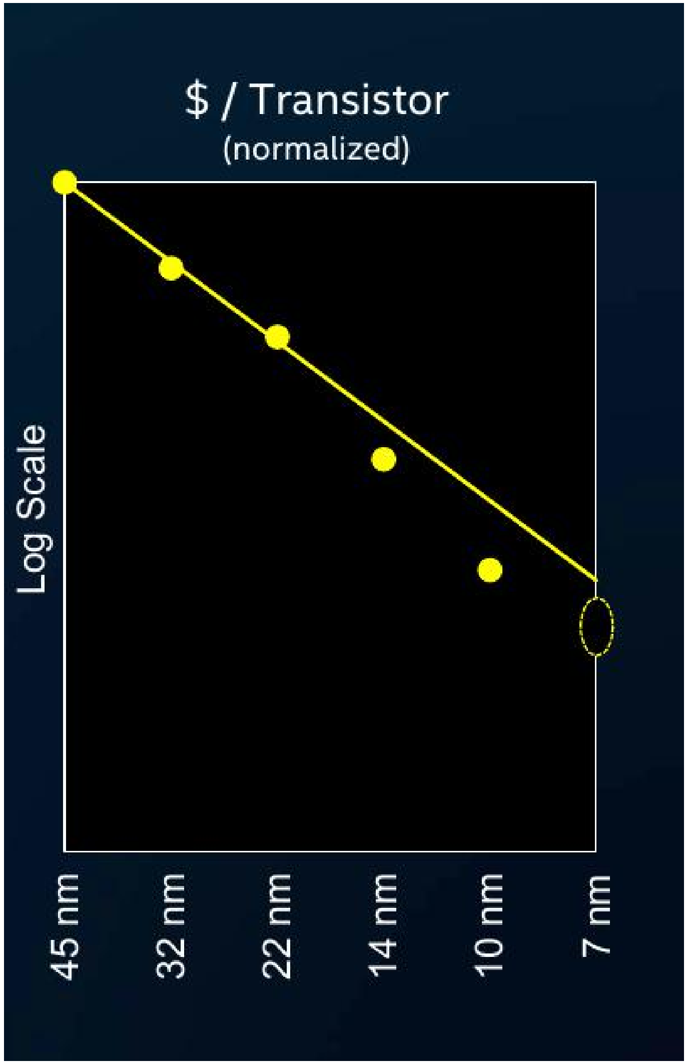
Moore and technology roadmap (ITRS)



	Year of Production	2013	2015	2017	2019	2021
1	Logic Industry "Node Name" Label	16/14	10	7	5	3.5
2	Logic ½ Pitch (nm)	40	32	25	20	16
3	FinFET Fin Half-pitch (new) (nm)	30	24	19	15	12
4	FinFET Fin Width (new) (nm)	7.6	7.2	6.8	6.4	6.1
5	FinFET Fin Width (nm) (*Detailed*)	6.4	5.3	4.4	3.7	3.1
6	6-t SRAM Cell Size(um2) [@60f2]	0.096	0.061	0.038	0.024	0.015
7	MPU/ASIC HighPerf 4t NAND Gate Size(um2)	0.248	0.157	0.099	0.062	0.039
8	4-input NAND Gate Density (Kgates/mm) [@155f2]	4.03E+03	6.37E+03	1.01E+04	1.61E+04	2.55E+04
9	450mm Production High Volume Manufacturing Begins (100Kwspm)			2018		
10	Vdd (High Performance, high Vdd transistors)[**]	0.86	0.83	0.8	0.77	0.74
11	1/(CV/I) (1/psec) [**]	1.13	1.53	1.75	1.97	2.1
12	On-chip local clock MPU HP [at 4% CAGR] (GHz)	5.5	5.95	6.44	6.96	7.53
13	Maximum number wiring levels [unchanged]	13	13	14	14	15
14	MPU High-Performance (HP) Printed Gate Length (GLpr) (nm) [**]	28	22	18	14	11
15	MPU High-Performance Physical Gate Length (GLph) (nm) [**]	20	17	14	12	10
16	ASIC/Low Standby Power (LP) Physical Gate Length (nm)	23	19	16	13	11

PRIZE EVOLUTION OF 1 Million transistors





Despite a strong increase of the complexity of the technology the price of a transistor still decreases due to the increase of density of transistors per chip.

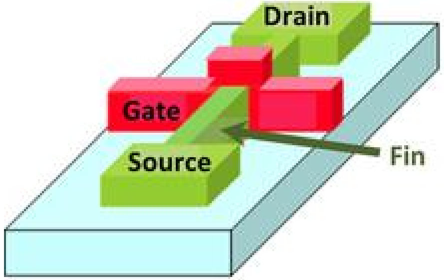
This constant evolution is possible because one uses a massive parallel fabrication process.

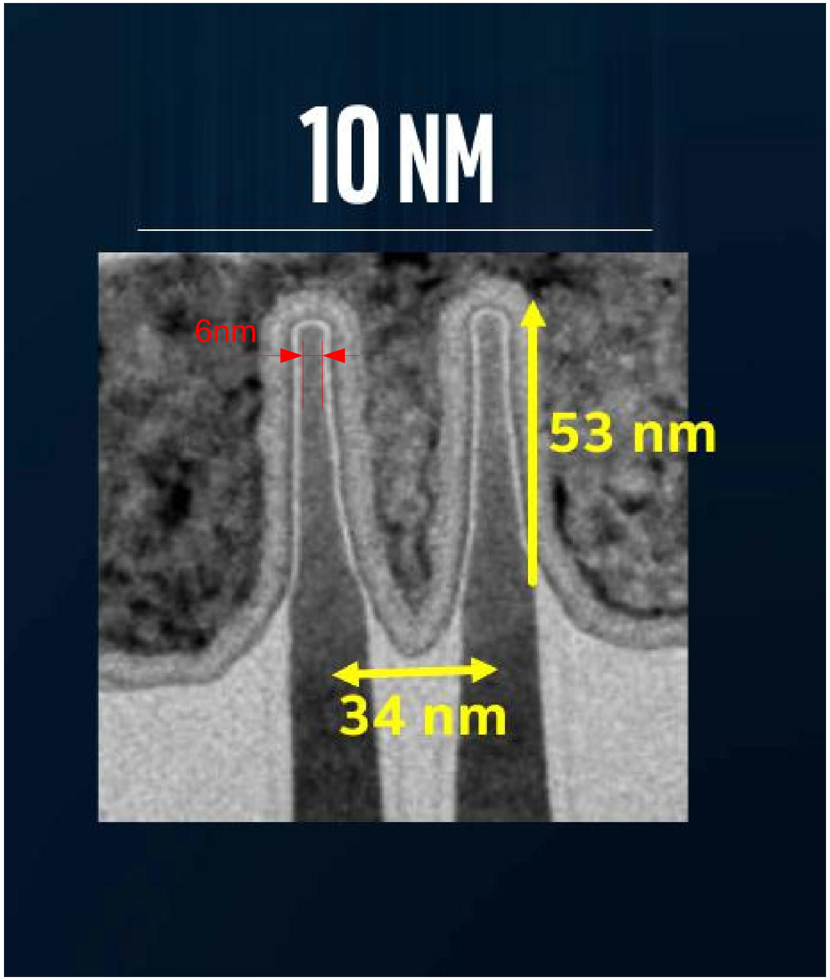
Impressive progress of optical lithography

For long time one believes that one can only reproduce features of the size of the wavelength that one uses. Resolution was limited to few hundred of nanometers

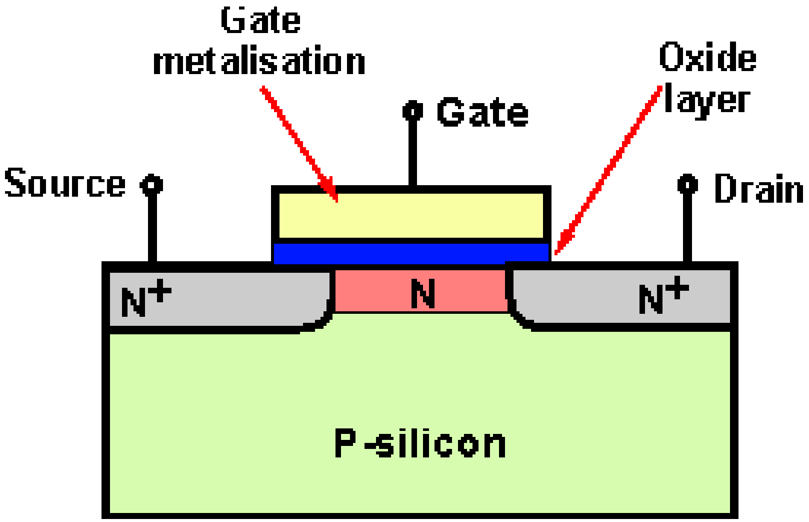
Currently the minimum size in an IC can be less then10nm !

Size of the Intel double fin-FET of the 10nm node (2017)





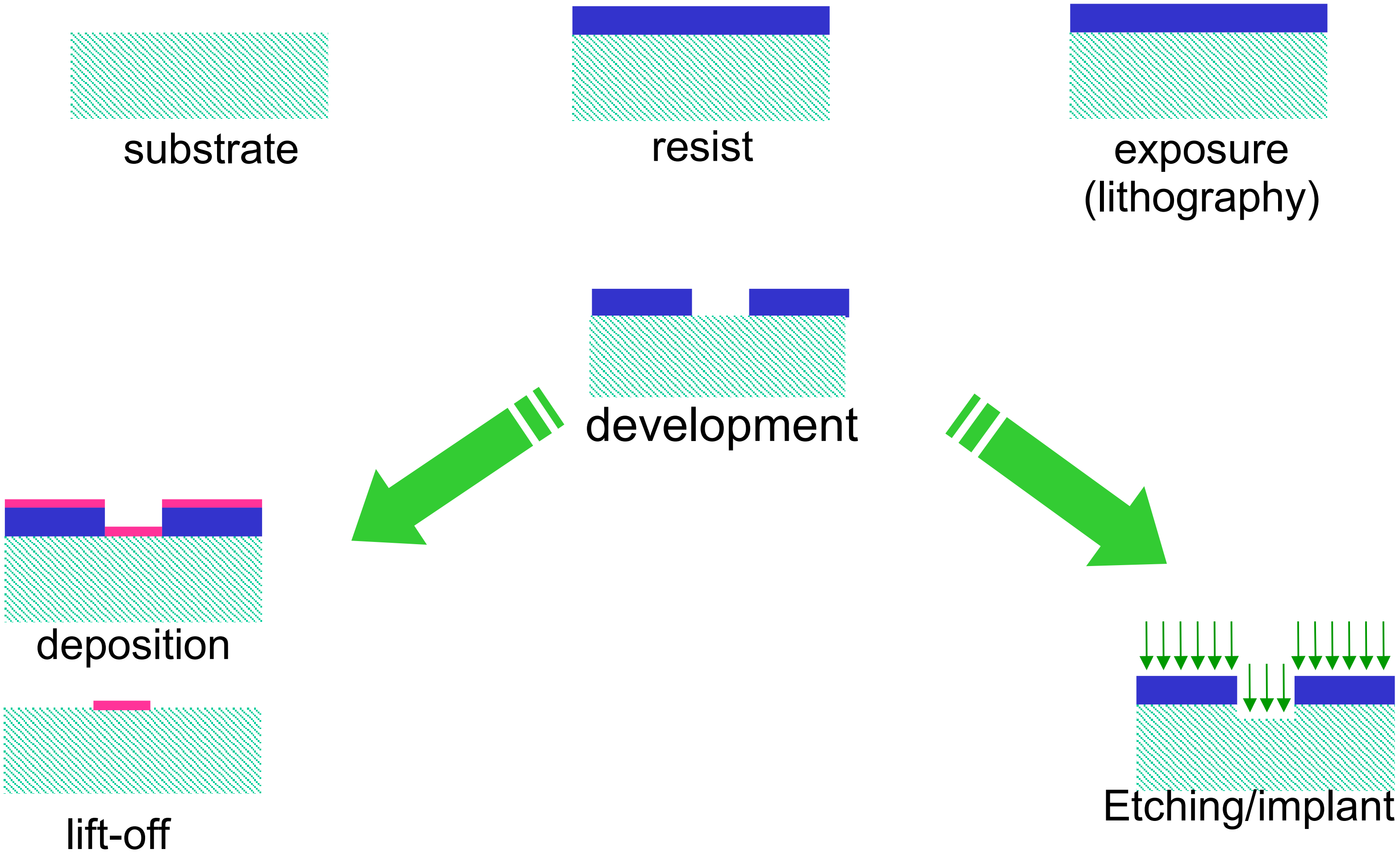
What are the main step of micro/nano fab



One needs to define a selected area where we can :
- Implant
- Deposit material
- Etch

The technique allowing to select a well defined area is called lithography

Typical process



substrate

resist

exposure
(lithography)

development

deposition

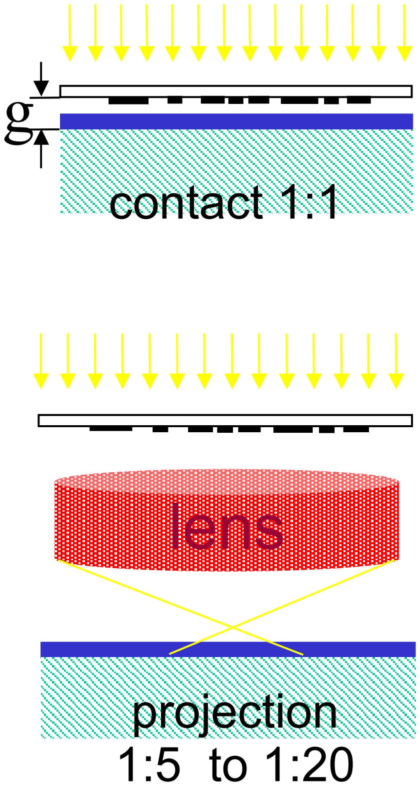
lift-off

Etching/implant

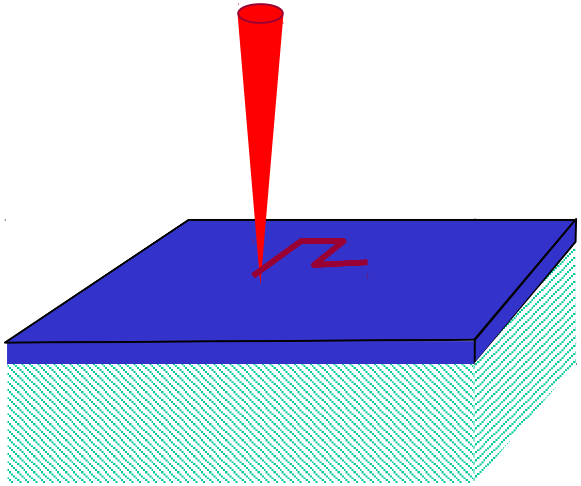
lithography

This is the crucial step that will define the size

optical



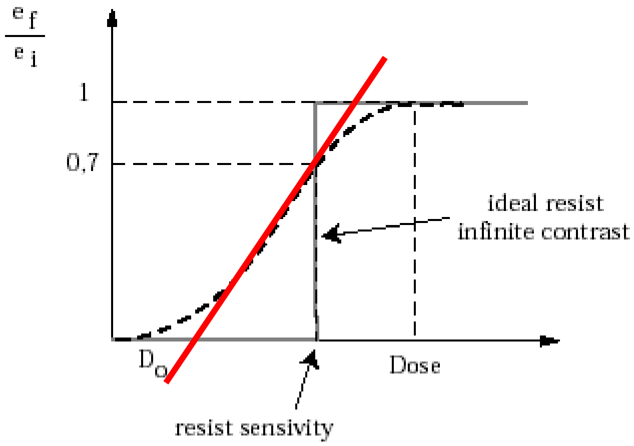
Focused beam



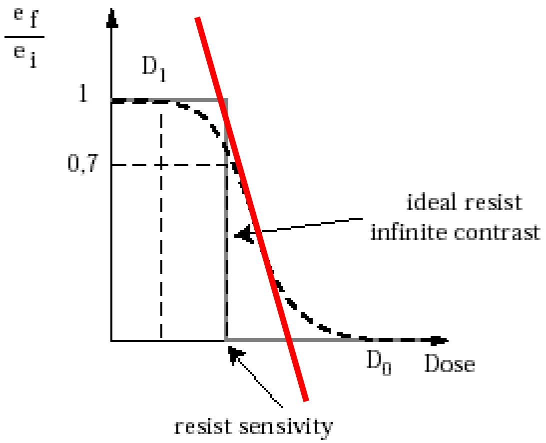
Nanoimprint
1:1

Resist and contrast

Most of the time we don’t want a nice gray scale but a very contrasted result.



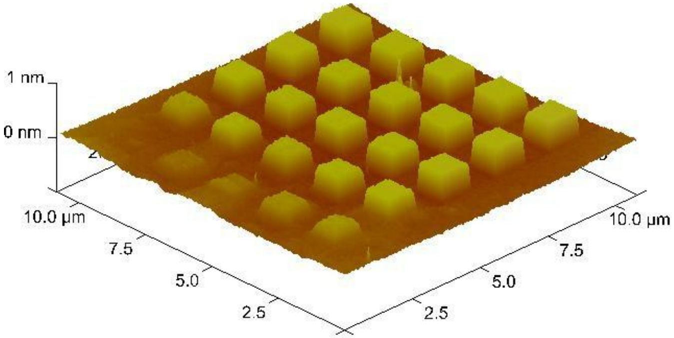
negative resist

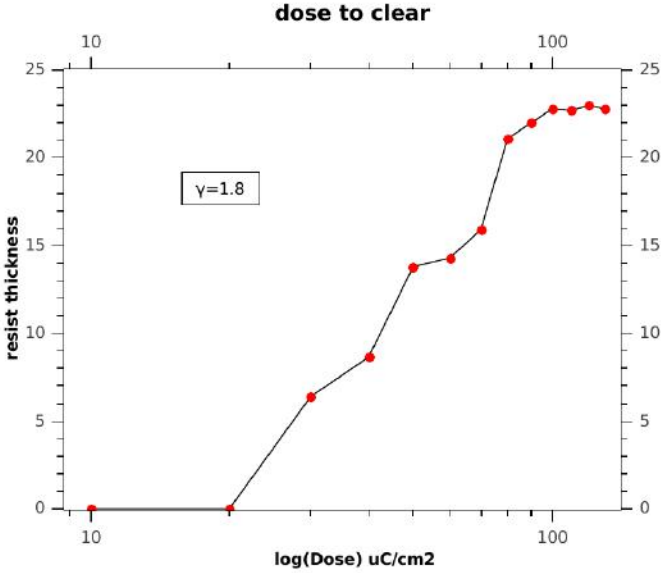


positive resist

Measurement of the contrast

One exposes aereas with increasing doses and measure the remaining height after development





Contrast curves strongly depend on the process : dose + developper + temperature (developper)

Optical lithography resists

- **Chemically amplified resist for a high sensitivity**
  - **catalyst acid is produced by the photon**
  - **Activated reaction: hydrolyse (positive resist), cross-link (negative resist)**

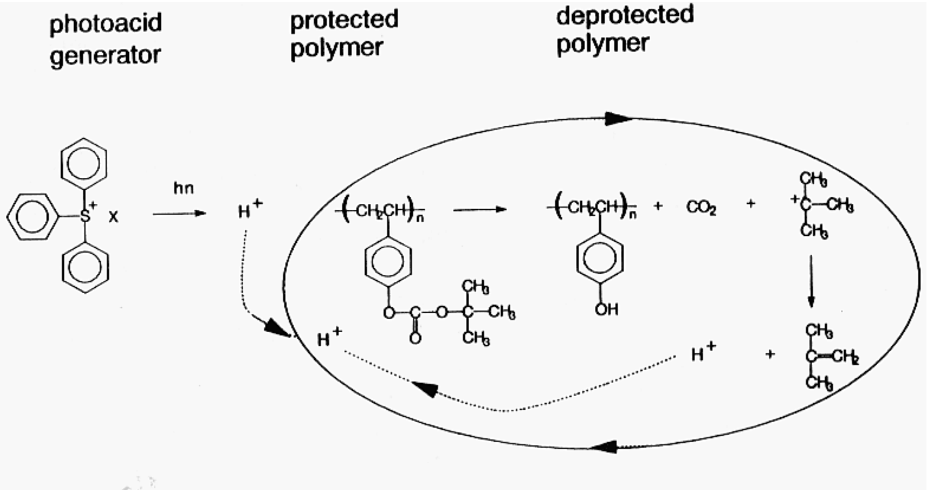
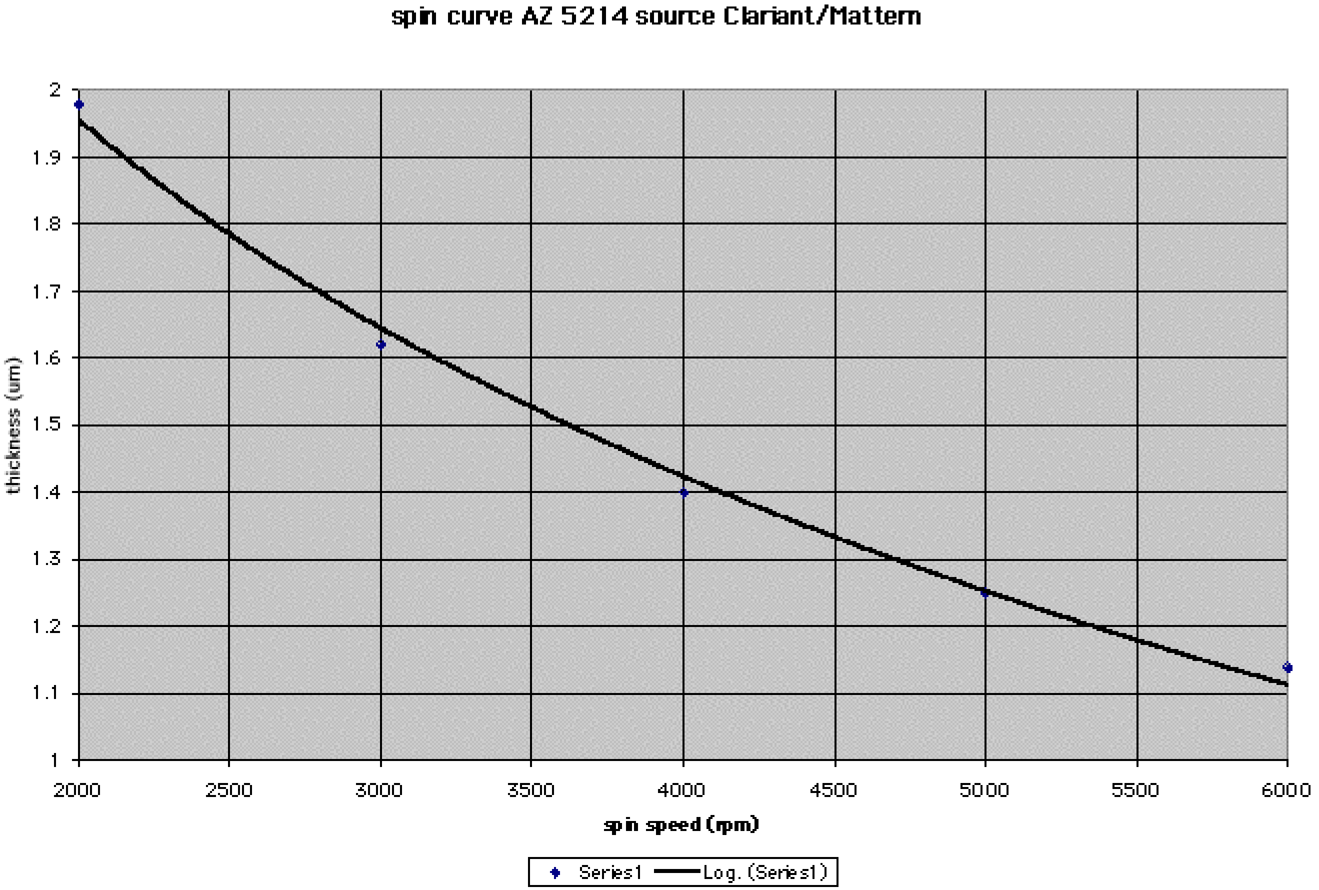


FIG. 4.4 Chemical amplification.

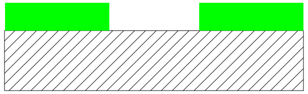
Spinning tool

To obtain a controlled flat film of resist one uses the centrifugal force

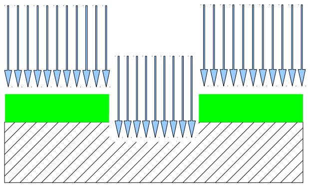
Resist spinning



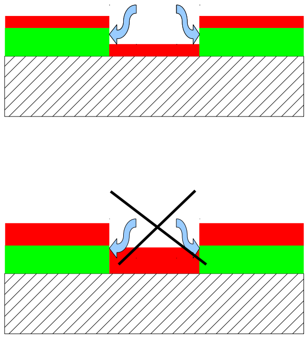
Resist thickness



Resist profile after litho+ development



Etching : depends on the differential rate of etching between resist and material



Metal deposition : lift off

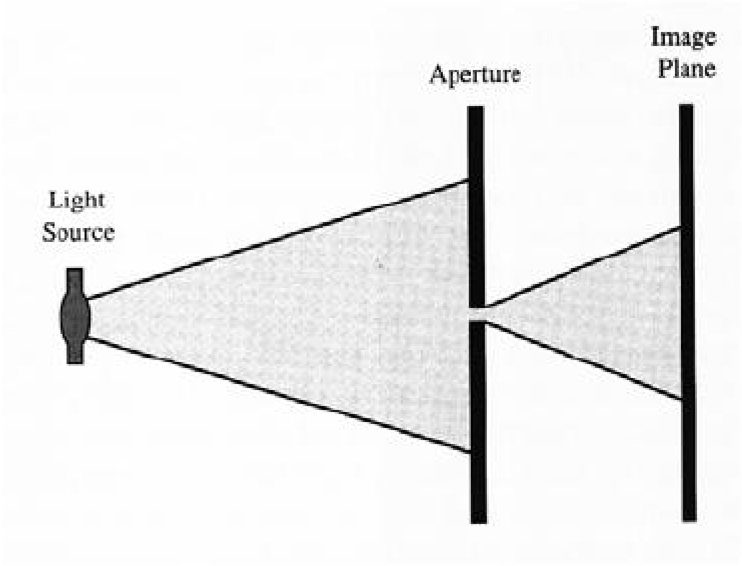
resist thickness ~3 x metal thickness

To have a safe solvent penetration

Optical lithography

Reminder on diffraction

- Diffraction

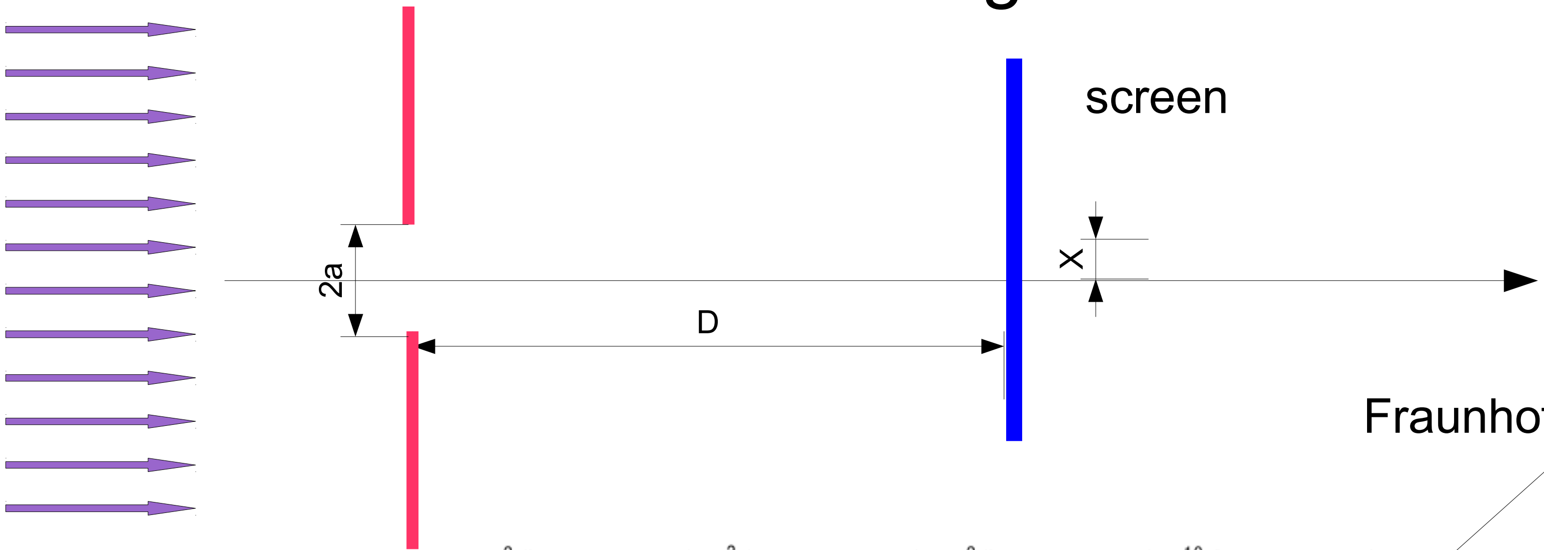


Diffraction : some intensity of light appears on masked area

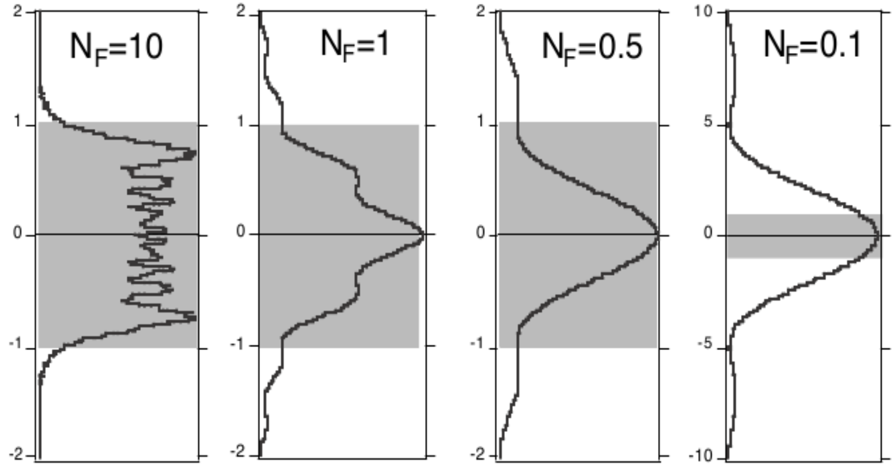
•Fresnel Diffraction : near field ; sphericlal waves

•Fraunhoffer Diffraction: far field ; plane waves

Diffraction through a slit



Fraunhoffer

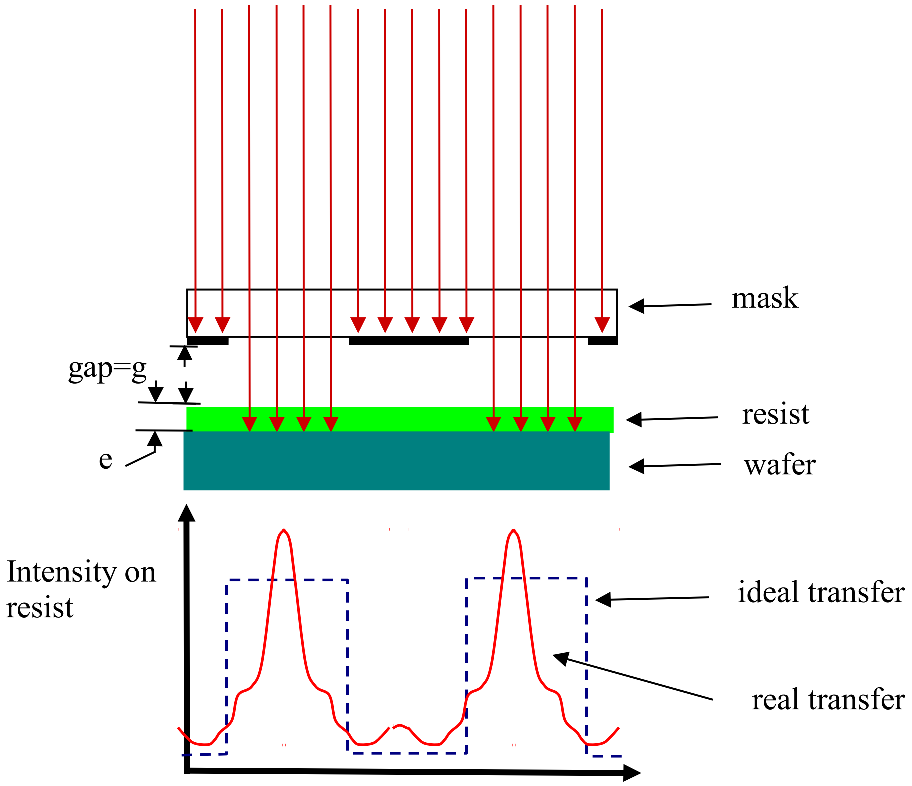


$$N_F = \frac{a^2}{\lambda D}$$

Fresnel Number

Fresnel

Optical lithography by proximity/contact



- resolution limited by Fresnel diffraction:

$$R \approx \sqrt{\lambda(g+e)}$$

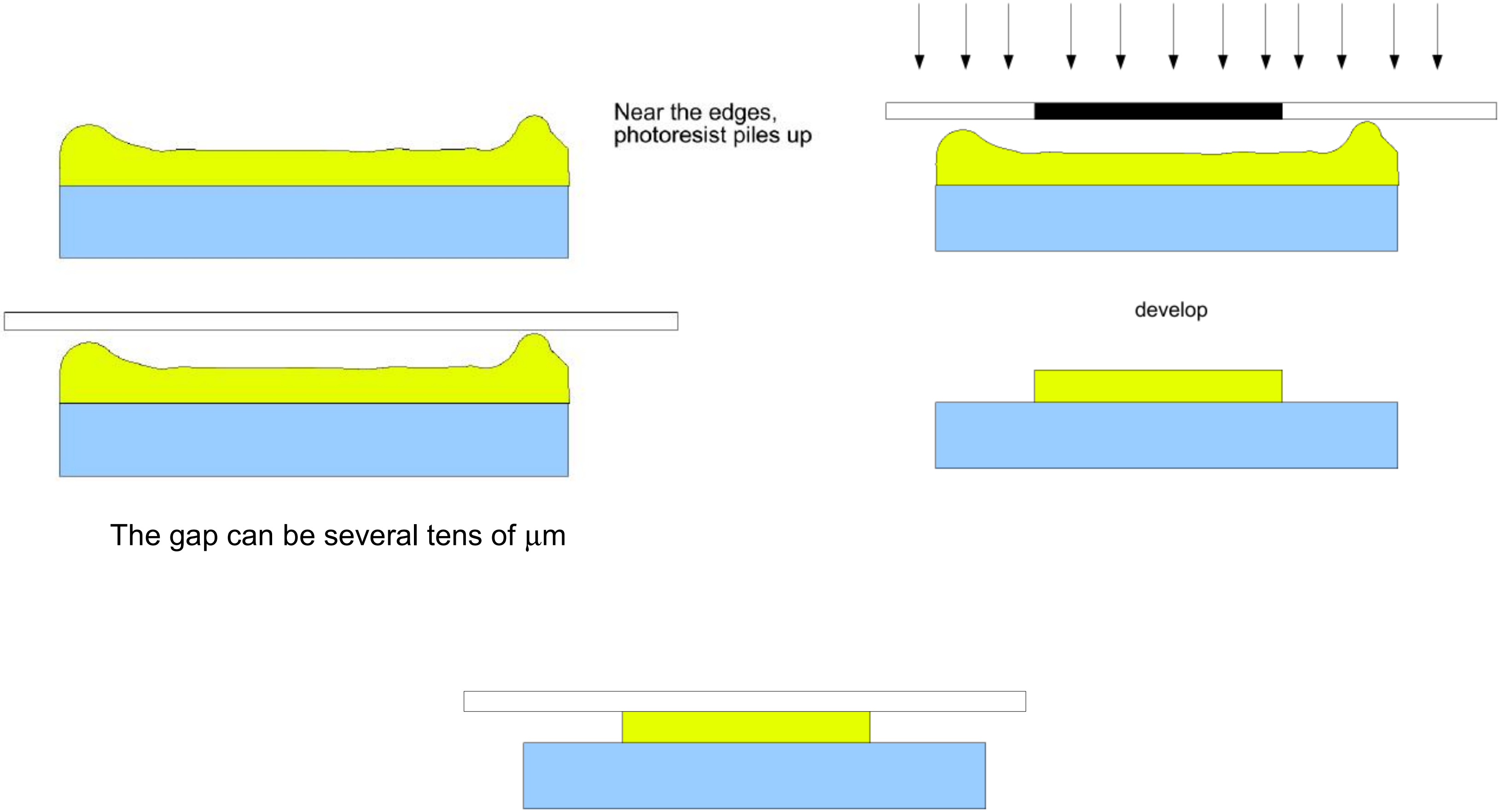
•Minimum gap= resist thickness

contact:

•Substrate flatness
•Resist damage
•Mask damage
•Masque 1:1

typically one can reach 0.5µm in contact mode
λ >157nm for mask transparency (heating)

Problem with edges



Near the edges, photoresist piles up

develop

The gap can be several tens of µm

The various wavelengths from Hg lamp

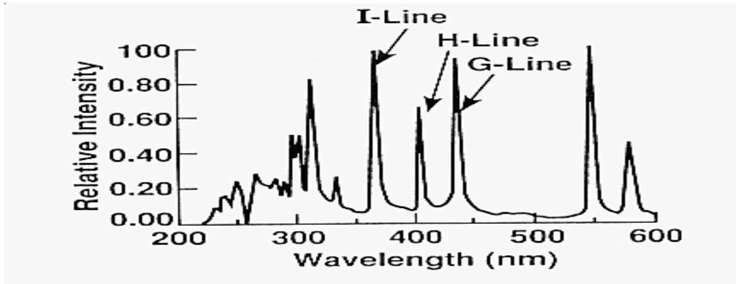
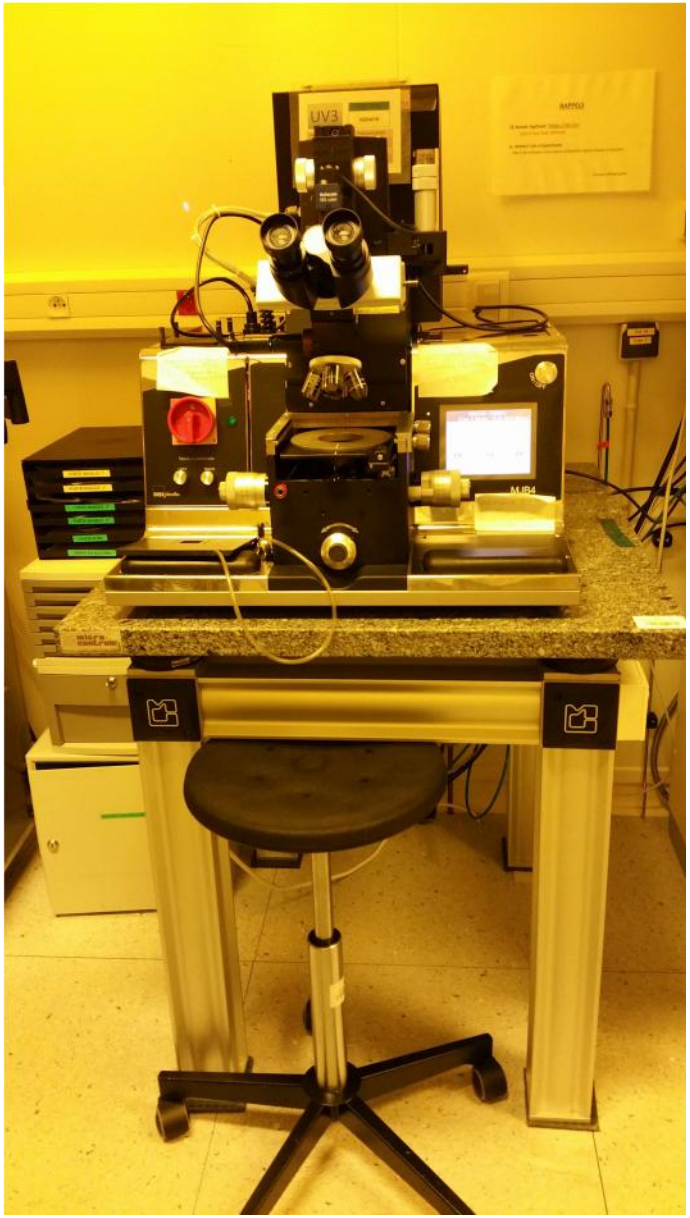


Figure 11. Typical high-pressure Hg-arc spectrum.

Mask :

Quartz plate of 4mm thickness (rigidity)

The pattern is realized by a selective etching of 80nm chromium

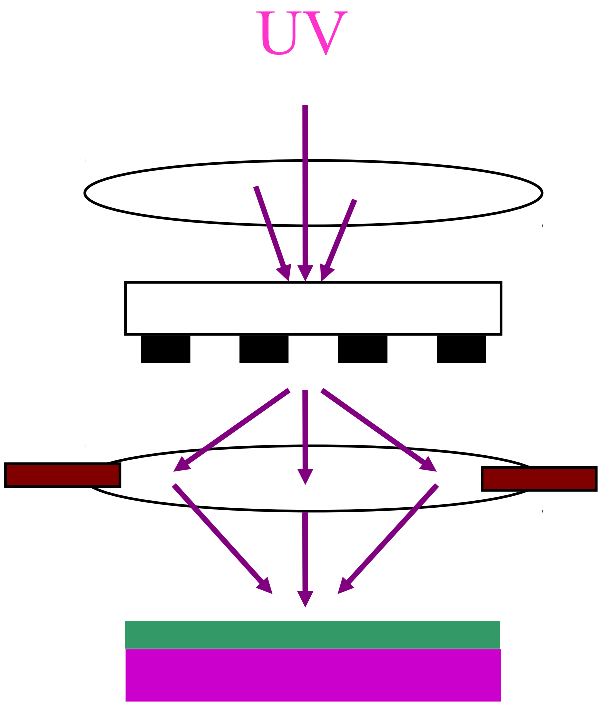


MA6 Karl Suss

Simple and economical technique it is well developed in lab and R&D

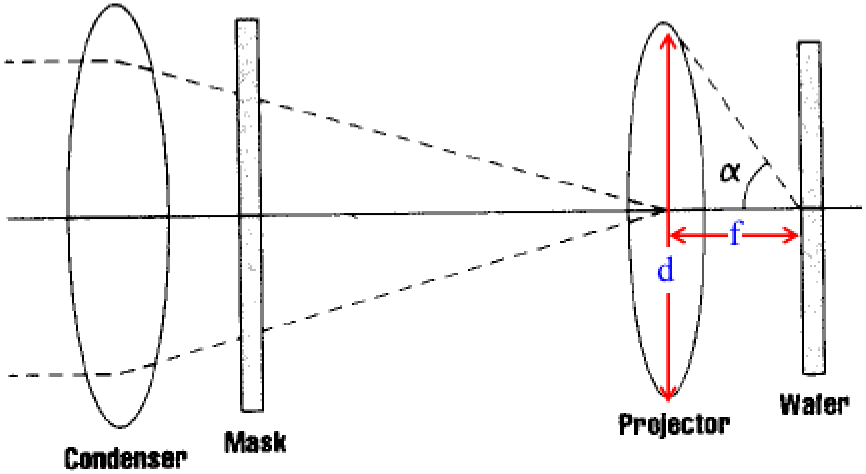
Projection lithography

A lens is used to project the image of the mask on the wafer



enlargment1:5 to 1:20

Numerical aperture



$$NA = n_o \sin\alpha$$

$$\mathbf{n}_0 = 1$$

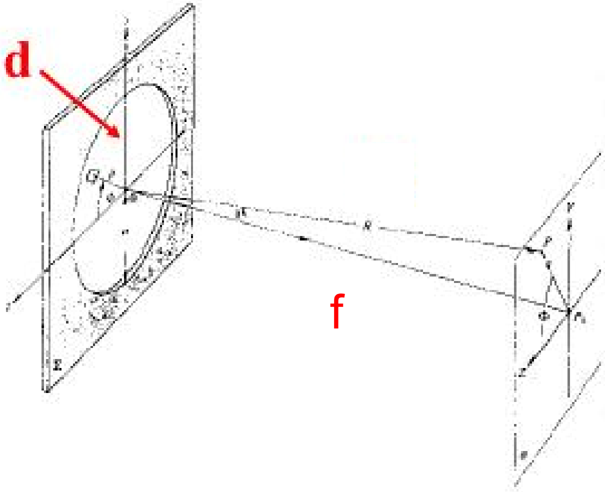
$$\sin\alpha \approx \frac{\mathbf{d}/2}{\mathbf{f}} = \frac{\mathbf{d}}{2\mathbf{f}}$$

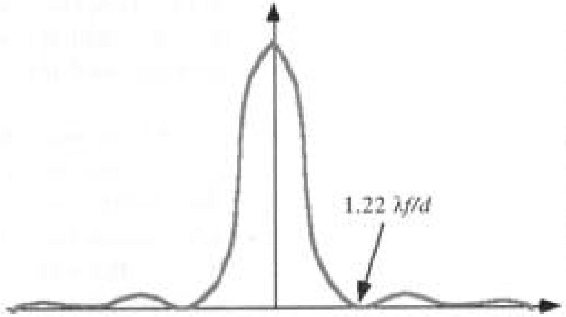
$$\mathbf{NA} = \frac{\mathbf{d}}{2\mathbf{f}}$$

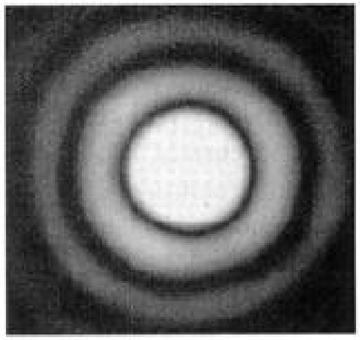
Numerical aperture is a measure of the capacity of the lens to capture light

α is the maximum angle that can be focused by the lens

Fraunhoffer diffraction of an aperture

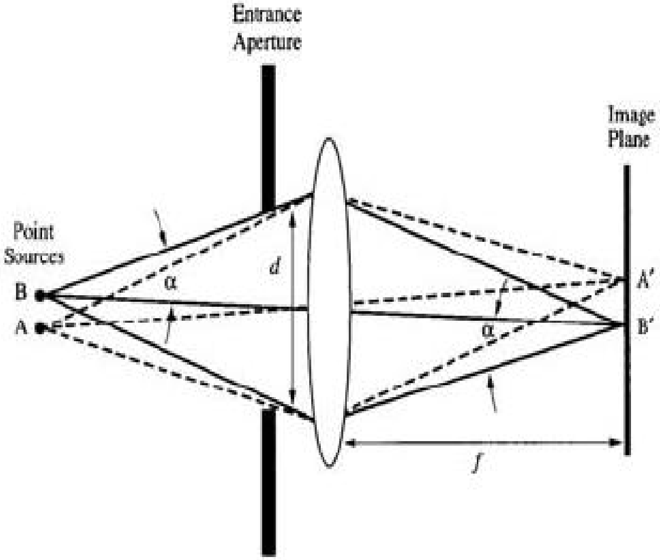


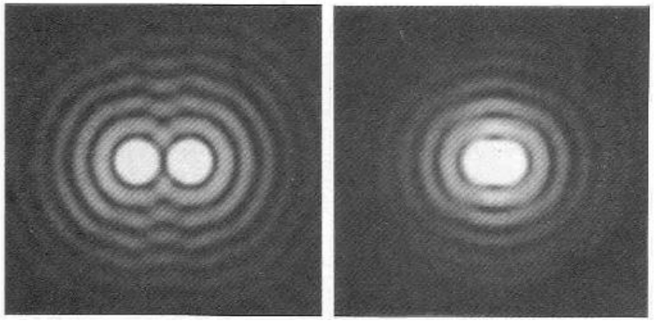


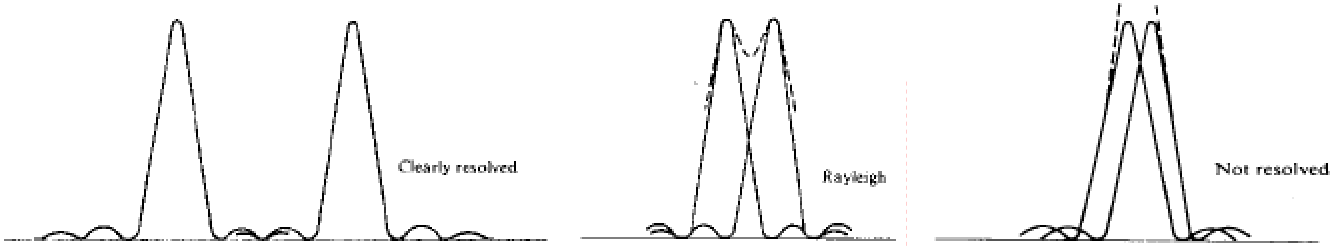


First minmum at x= 1.22 λf/d

resolution





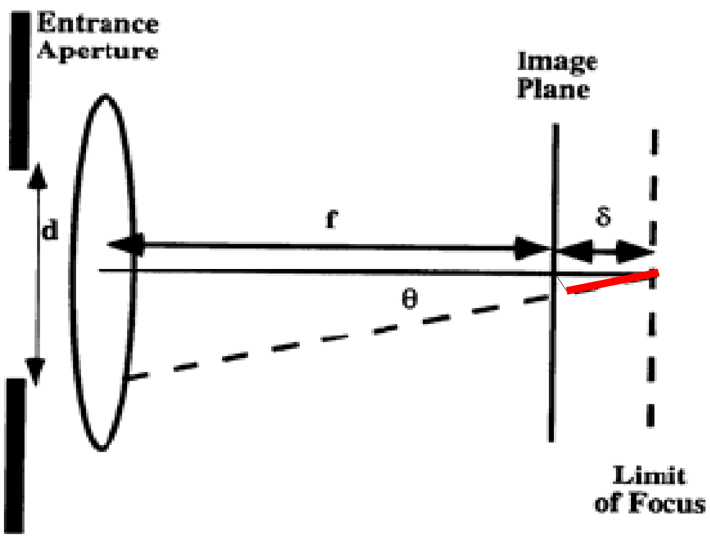


$$(\Delta l)_{\min} = 1.22\frac{R\lambda}{2a} = 1.22\frac{f\lambda}{d}$$

$$(\Delta I)\min = 0.61\frac{\lambda}{NA} = k\frac{\lambda}{NA}$$

k is a technological parameter which is theoretically 0.61 but progresses will scaled it down

Depth of focus



The depth of focus decrease when NA increases in conflict with the resolution.

Raleigh criteria for DOF : change in optical path between the zero order diffraction (on the optical axis) and the one by the edge of the aperture $=\lambda/4$

$$\frac{\lambda}{4}=\delta-\delta\cos(\theta)=\delta(1-\cos(\theta))$$

$$\cos(\theta)\approx 1-(\theta)^2/2 \quad \text{small} \quad \theta$$

$$\sin(\theta)\approx\theta$$

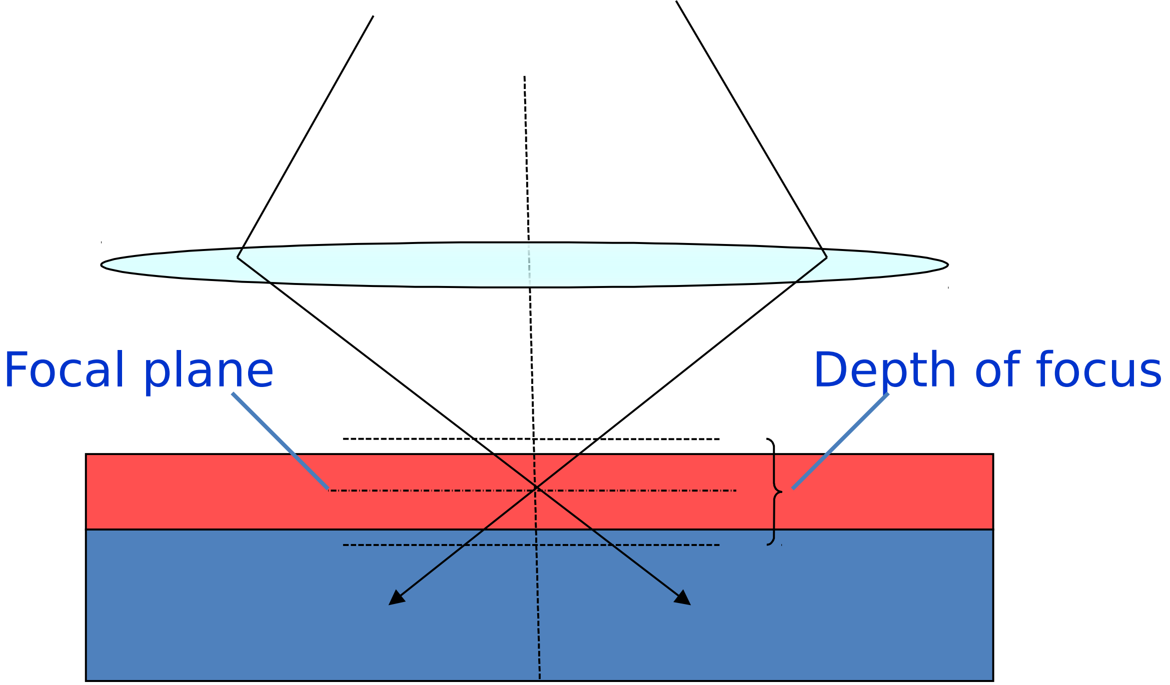
$$\frac{\lambda}{4}=\delta\frac{(NA)^2}{2} \qquad DOF=\frac{\lambda}{2NA^2}$$

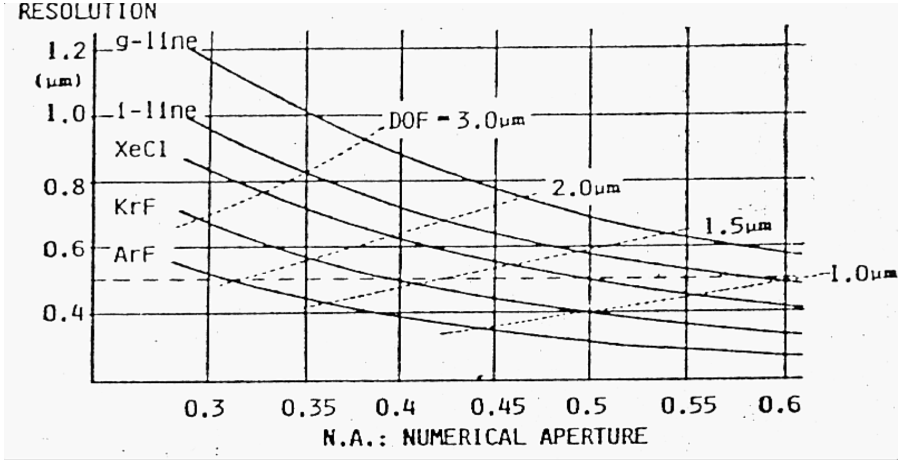
Importance of the DOF:
Flatness of the substrate
Previous technological steps can give various heights

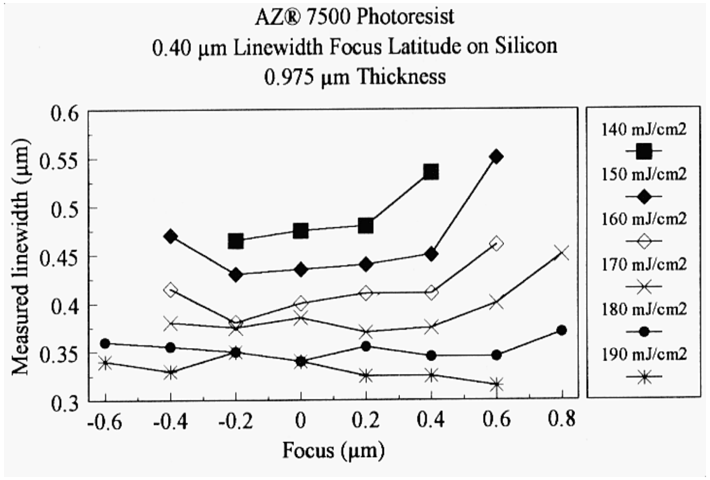
$$DOF=k_2\frac{\lambda}{NA^2}$$

Optimal focal plane in photolithography

- Light should be focused on the middle point of the resist layer.
- In IC, DOF is << 1μm, hard to focus if wafer is not super flat.
- People talks more of resolution, but actually DOF can often be a bigger problem than resolution.
- For example, a 248nm (KrF) exposure system with a NA = 0.6 would have a resolution of ≈0.3μm (k_1 = 0.75) and a DOF of only ≈ ±0.35μm (k_2 = 0.5).







résolution, NA, λ and DOF **resolution vs focus and dose (i-line, NA=0.54)**

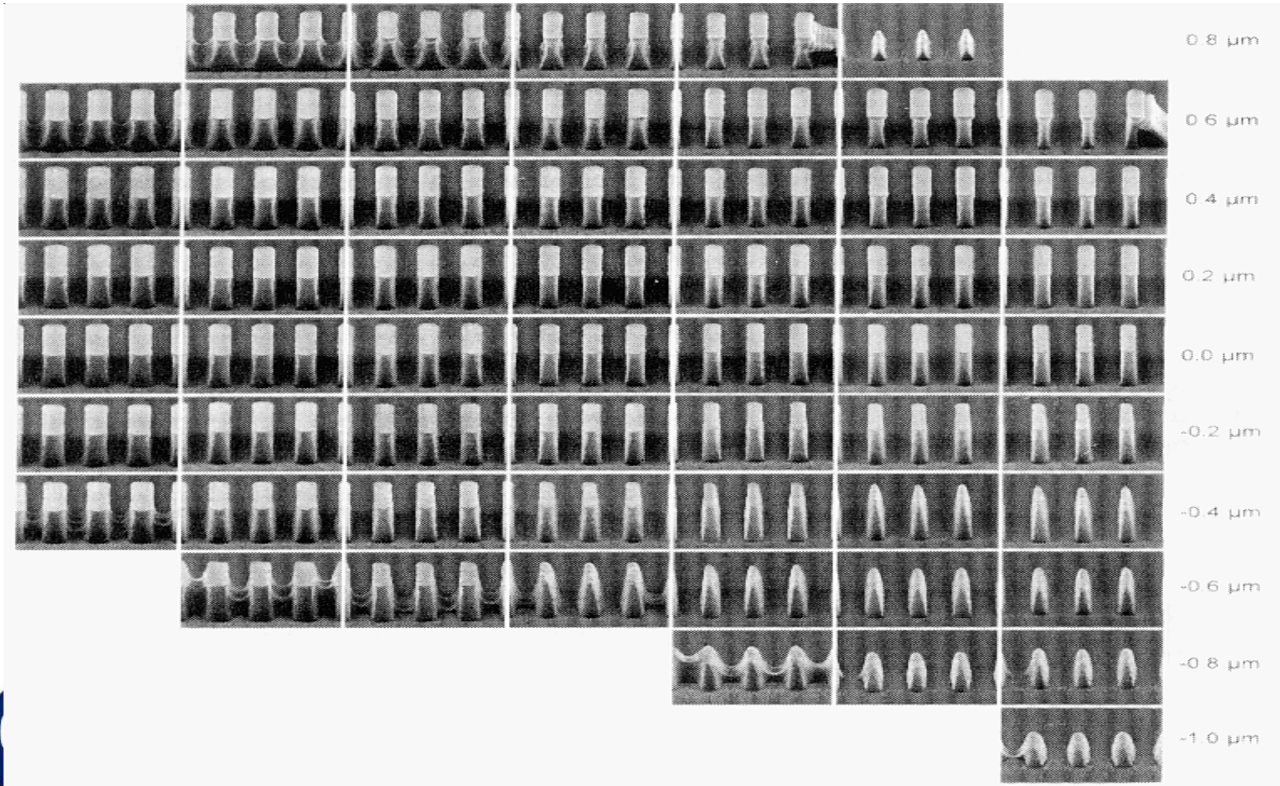


FIG. 1.31 Resist profiles for imaging at best focus and outside the depth of focus[80].

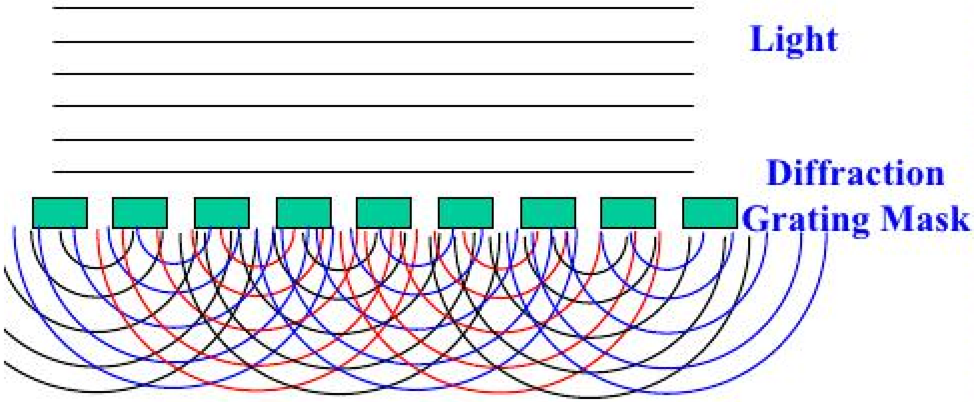
DOF effect on exposure: profile in the resist upon varying the focus (y) and the dose (x)

The process latitude is strongly affected by the DOF

Modulation Transfer Function (MTF)

One defines the ModulationTransfer Function :

$$MTF = \left[\frac{I_{\max} - I_{\min}}{I_{\max} + I_{\min}} \right]$$

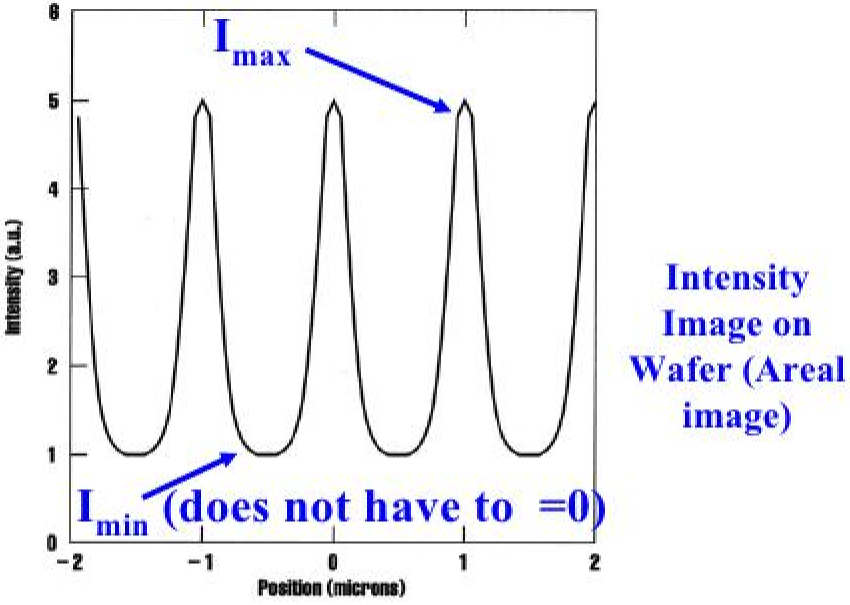


MTF is a measure of the ability of the optical system to modulate the intensity of the light on the wafer

.

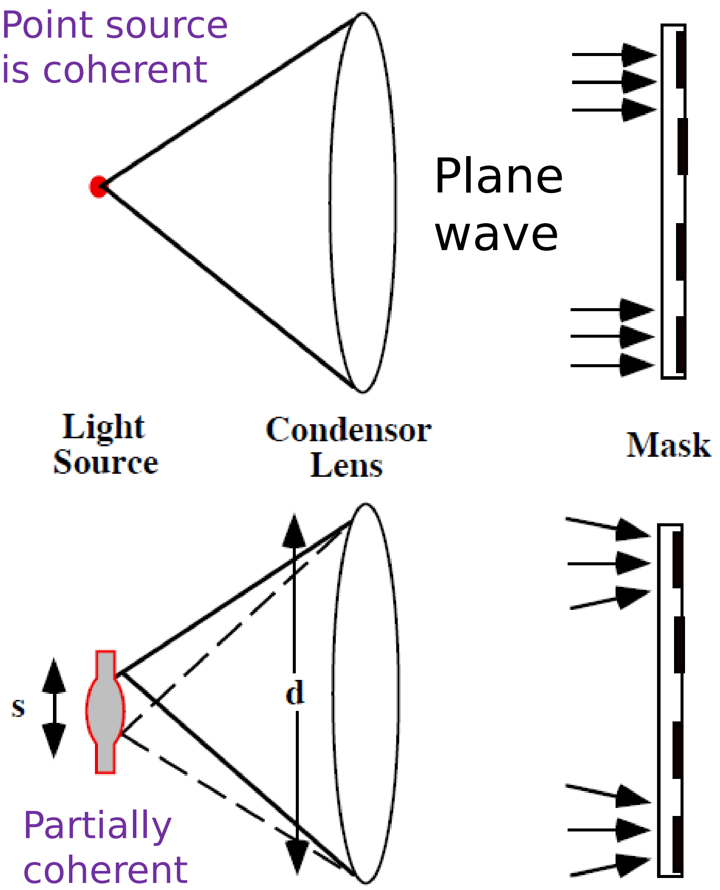
The smaller the period of the grating the bigger are diffraction effect and the MTF decreases.
Usually MTF > 0.5 is preferred.
It depends on λ, light source size (coherency), and optical system.

Importance of the resist contrast



MTF and spatial coherence

Spatial coherence of light source



Point source is coherent

Plane wave

Partially coherent

- Coherent light will have a phase to space relationship.
- Incoherent light or light with only partial coherence will have wave-fronts that are only partially correlated.
- Spatial coherence S is an indication of the angular range of light waves incident on mask, or degree to which light from source are in phase.
- Small S is not always good (see next slide).

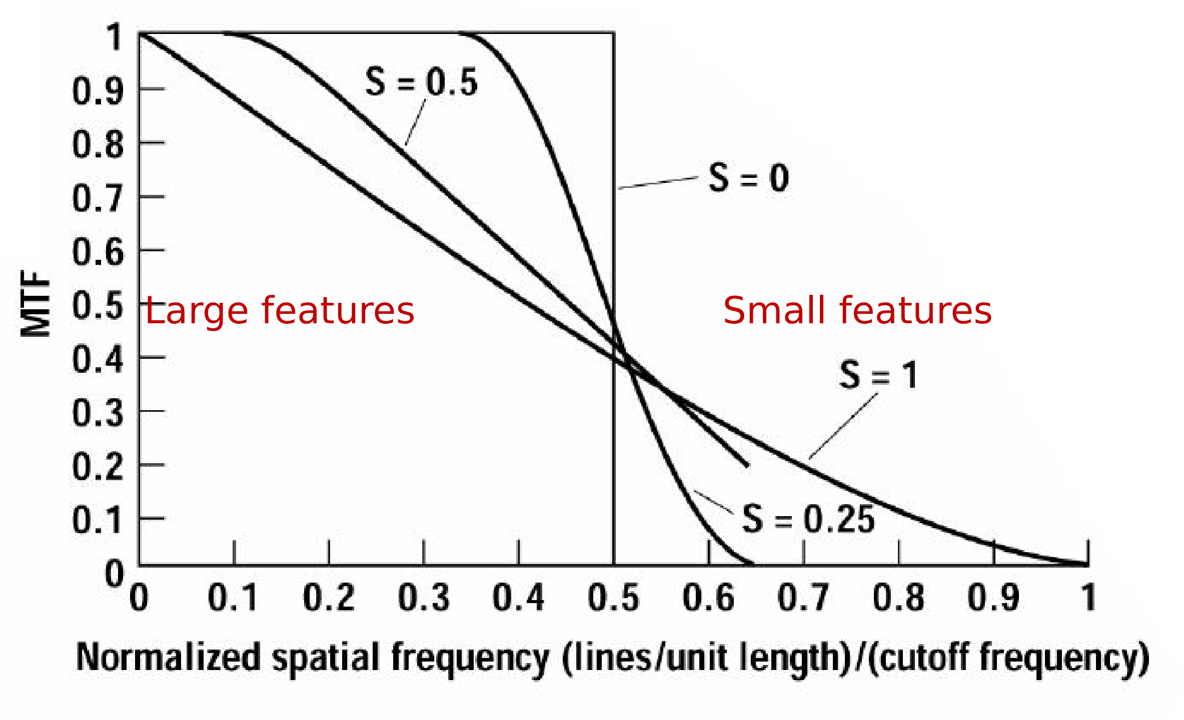
$$S = \frac{\text{source diameter}}{\text{aperture diameter}} = \frac{s}{d}$$

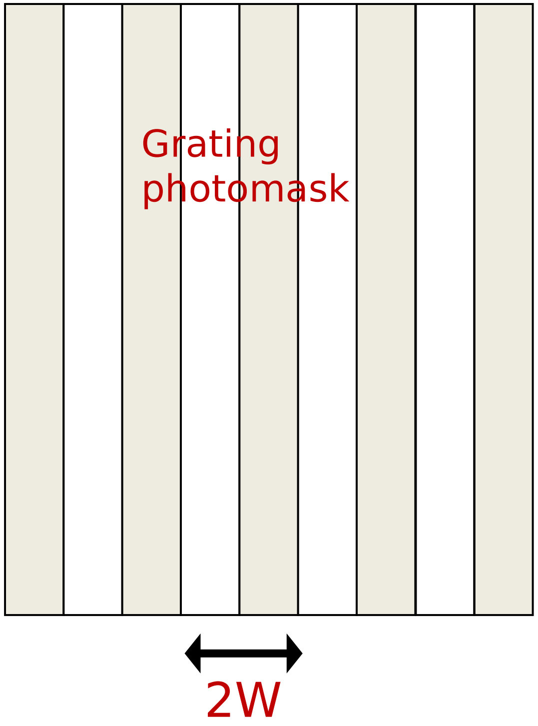
MTF and spatial coherence

MTF vs. diffraction grating period on mask.

W = line width

X-axis of the plot: spatial frequency $\nu=1/(2W)$, normalized to Rayleigh criterion cutoff frequency $\nu_0=1/R=NA/(0.61\lambda)$.





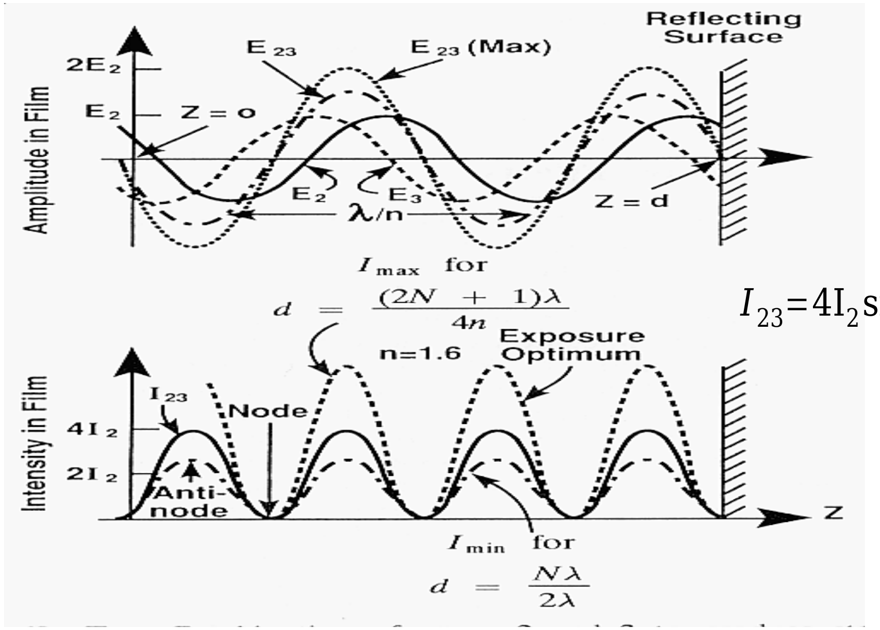
For a source with perfect spatial coherence S=0, MTF drops abruptly at Rayleigh criterion W=half pitch=R=$k_1\lambda$/NA.

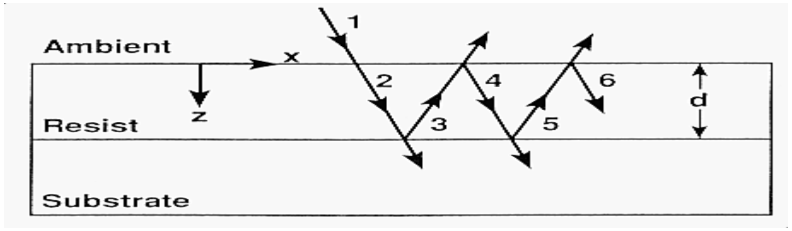
Large S is good for smaller features, but bad for larger ones.

Trade-off is made, and industry chooses S=0.5-0.7 as optimal.

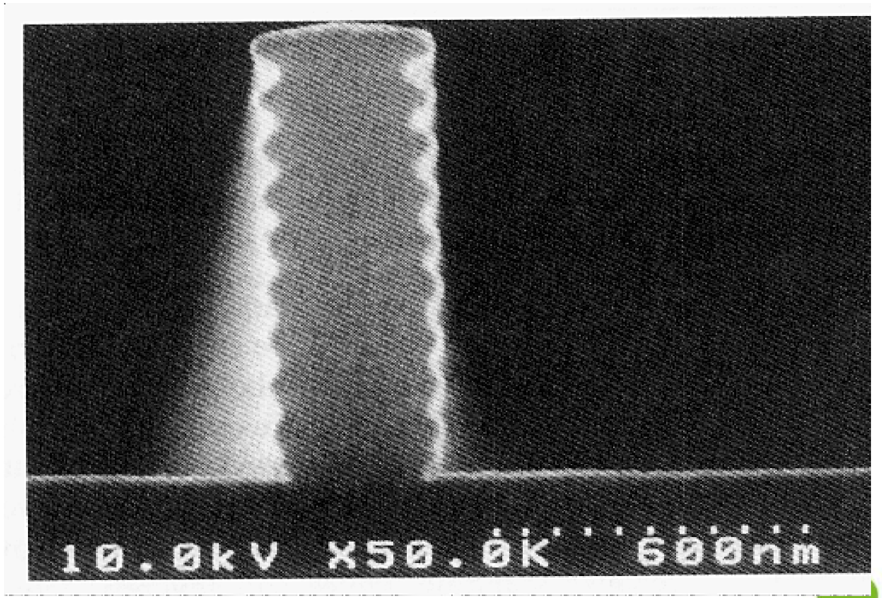
Interference effects in the resist

Constructive and destructive interference between incident and reflected light results in a periodic intensity distribution across the resist thickness.





$$I_{23} = 4I_2 \sin\left[k(d-z)\right]$$



Solutions:

Anti Reflecting Coating (ARC)

Optical lithographie

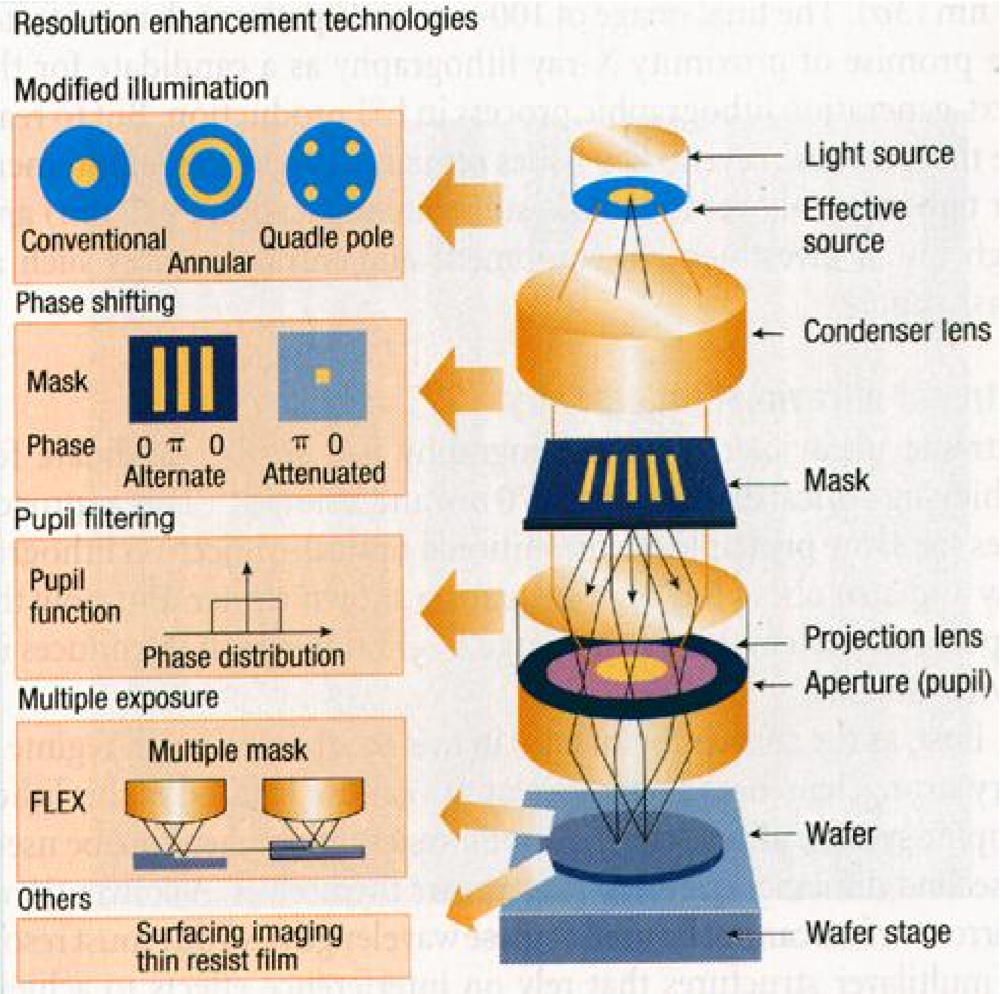
Year	λ	N.A.	resolution	k
1980	436nm	0.28	1.25µm	0.8
1990	365nm	0.48	0.5µm	0.65
1995	248nm	0.5	0.3µm	O.6
1999	248nm	0.63	0.18µm	0.46
2004	193nm	0.6	0.090µm	0.49
2010	193nm	1.35	0.045µm	0.27

$k<k_{Rayleigh}$ by use of tricks: top imaging technique , phase shift mask, double exposure , off axis ... (RET)

Decreasing wavelength

- When decreasing λ, one increases the absorption of materials.
- Below 193nm it is difficult to find a transparent material without absortion
- Absorption means temperature increase
- Temperature increase means dilatation
- In microelectronics 193nm is the limit for projection lithography
- A new option is EUV lithography with λ=13.5nm without lens

RET (Resolution Enhance Technologies)



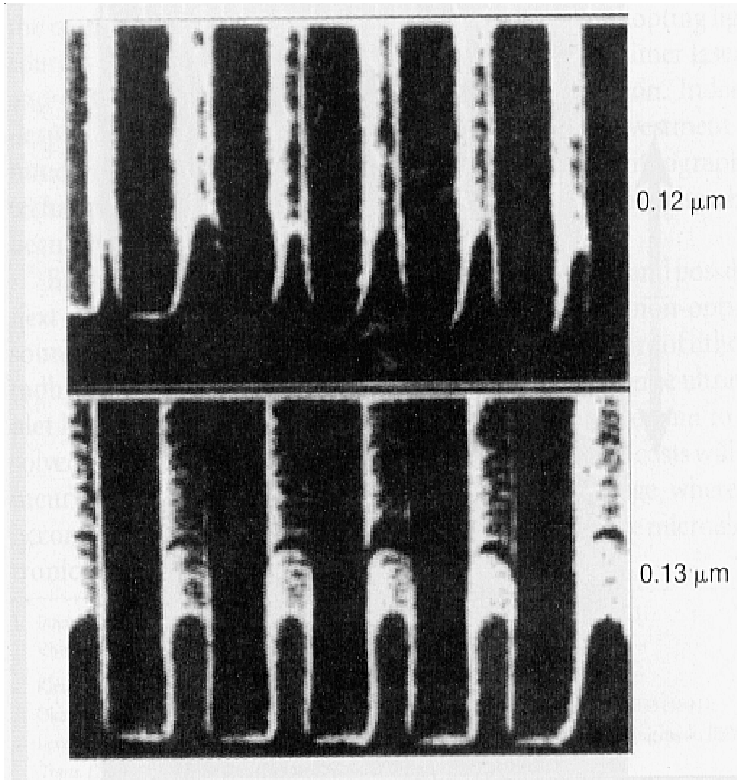
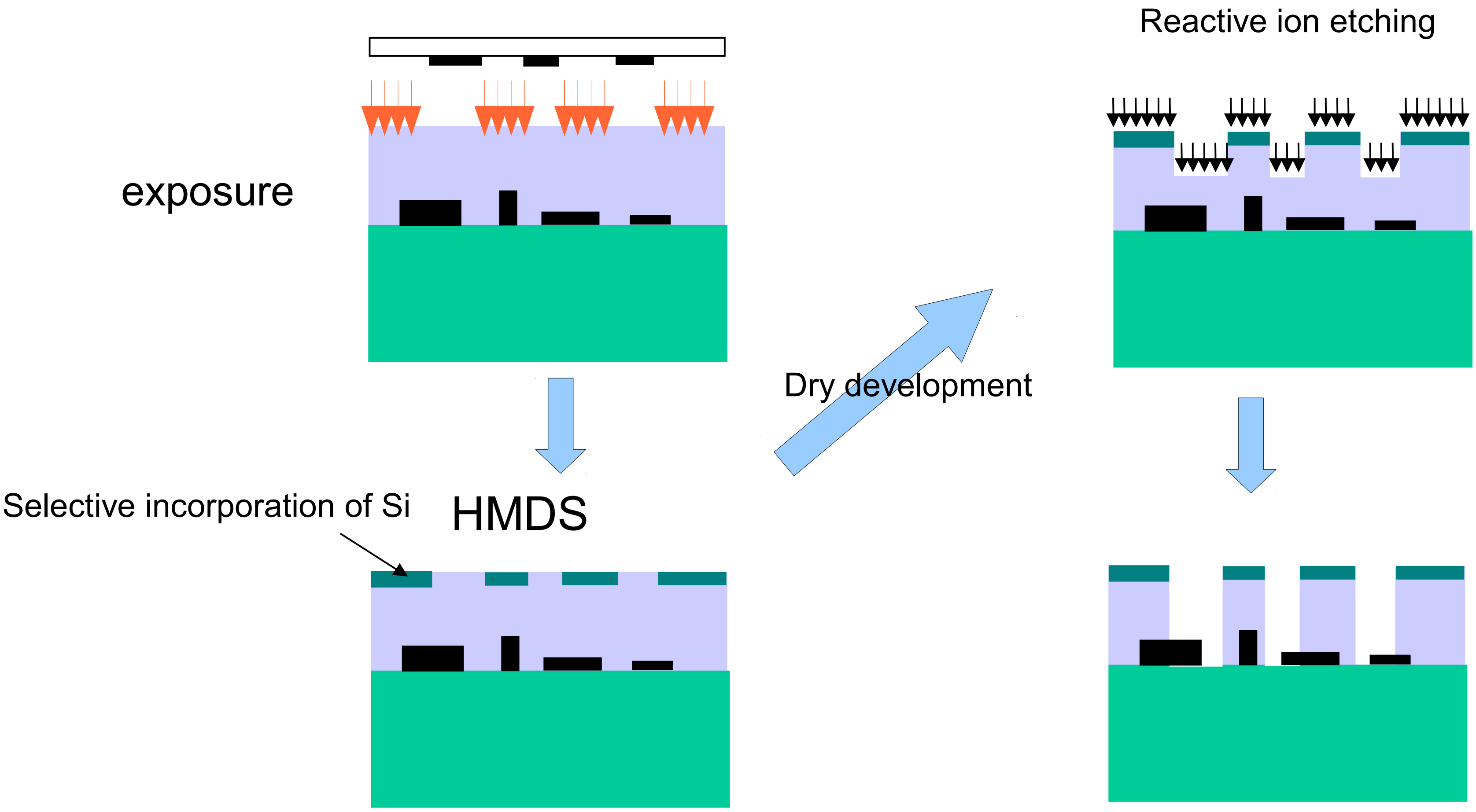


Figure 5 An example of resolution enhancement using phase-shifting technology. The exposure system uses a KrF excimer laser ($\lambda = 0.248$ µm; NA = 0.55; $\sigma = 0.3$). Structures having half the wavelength of the exposure light are clearly visible.

Top imaging technique



exposure

Selective incorporation of Si

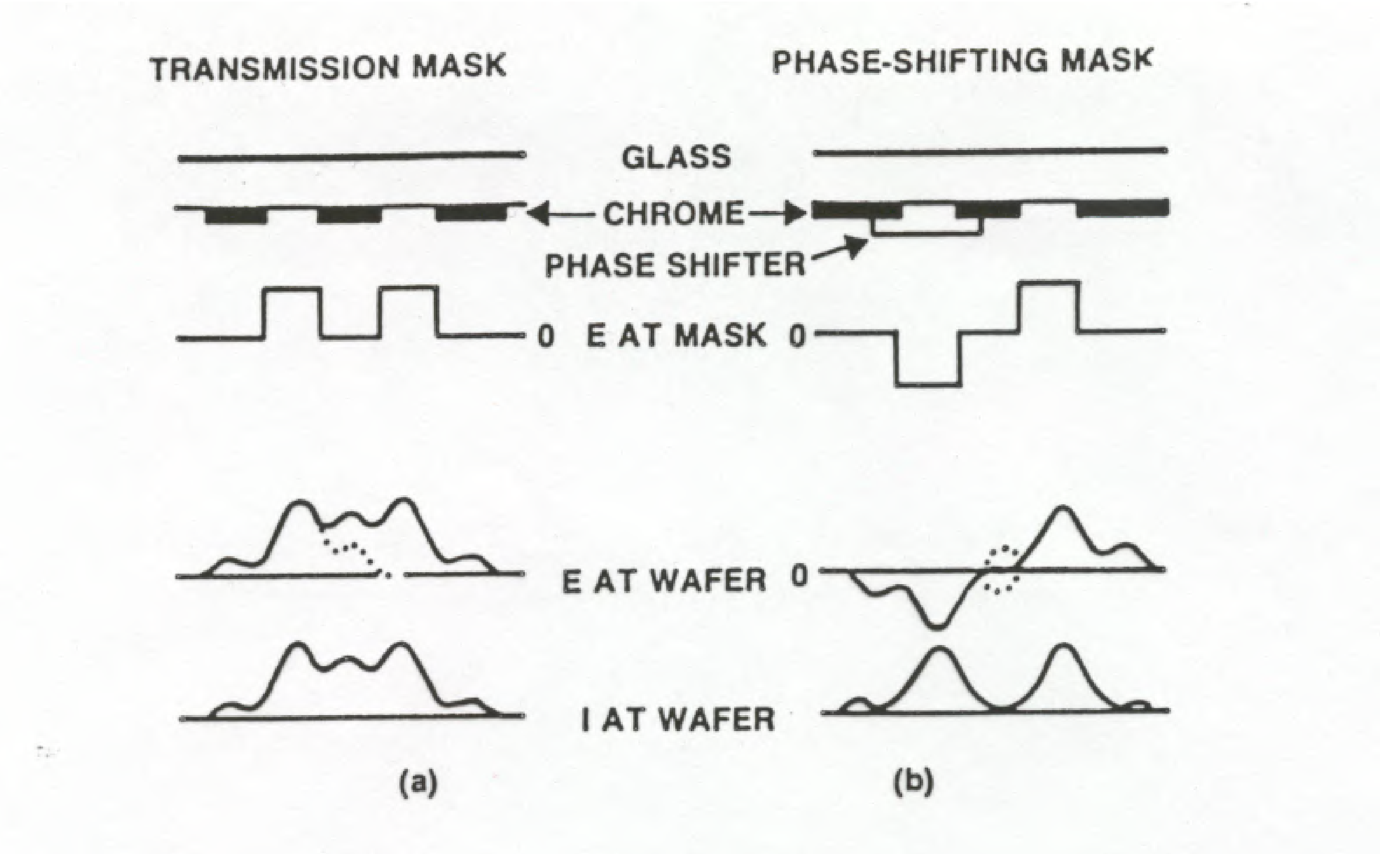
HMDS

Dry development

Reactive ion etching

Not sensitive to DOF, interference in resist, planarisation

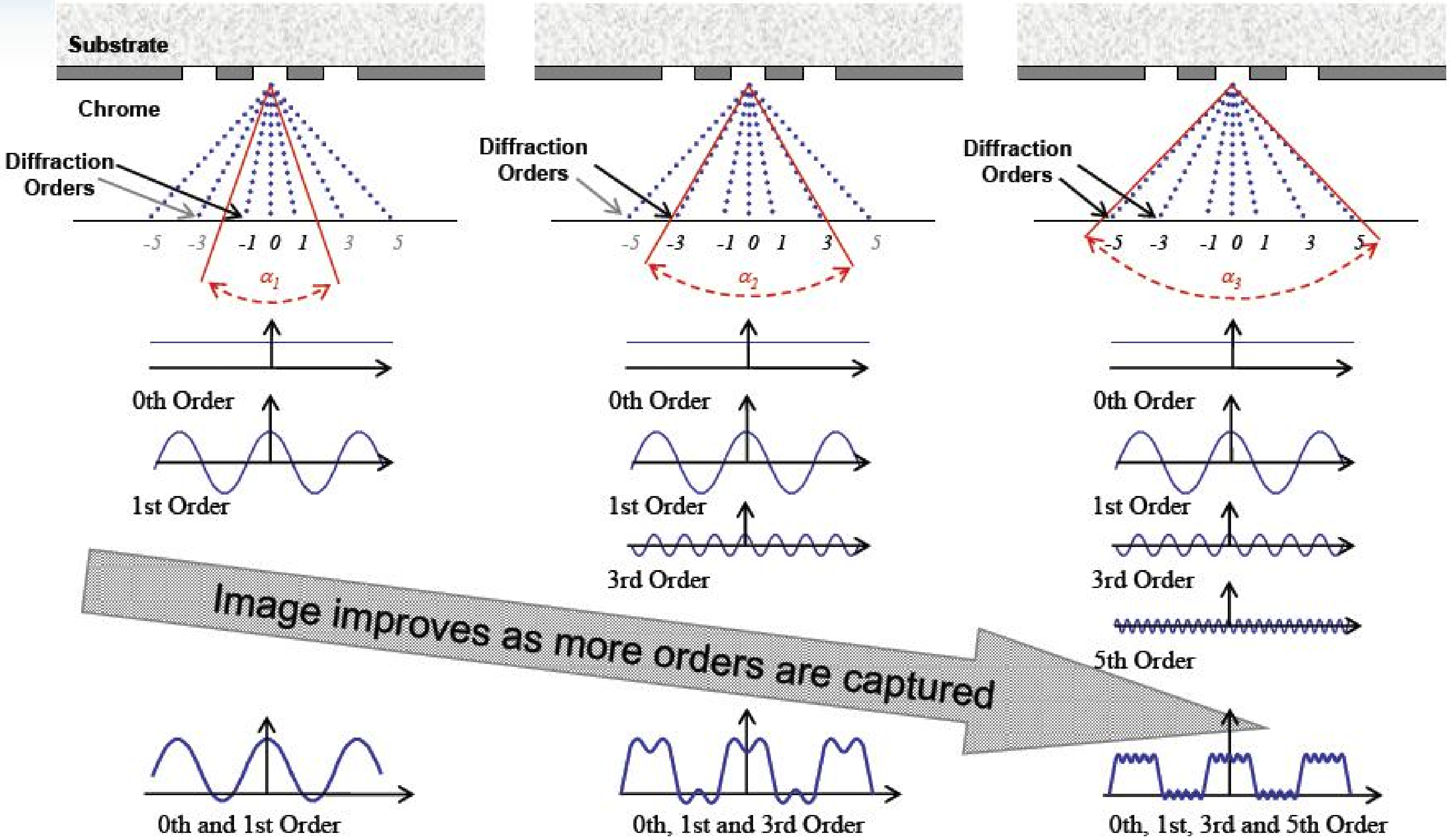
Phase shifting mask



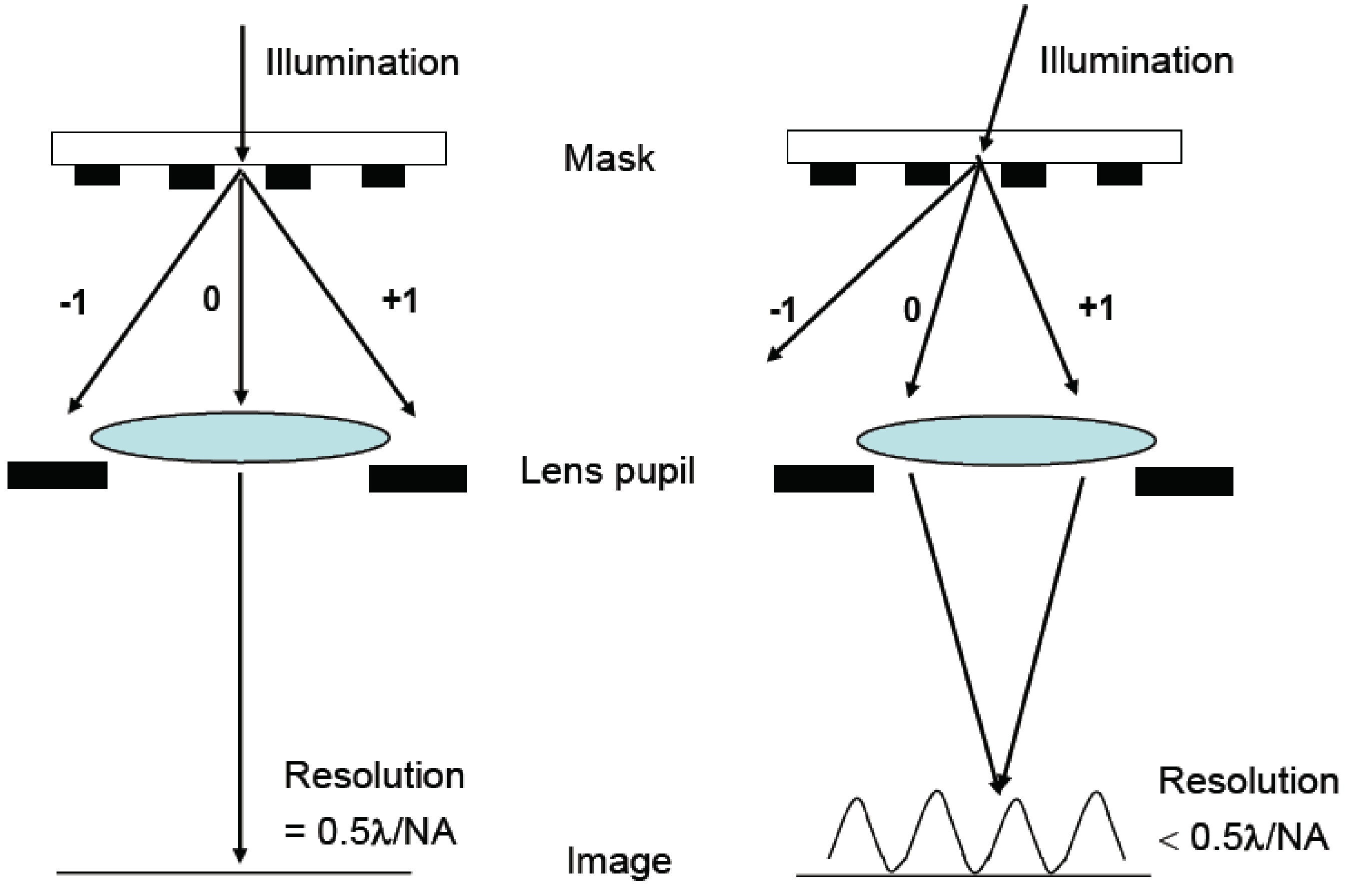
$k_1 : 0.61 \longrightarrow 0.4$

Mask more complex → price!!

Image Capture

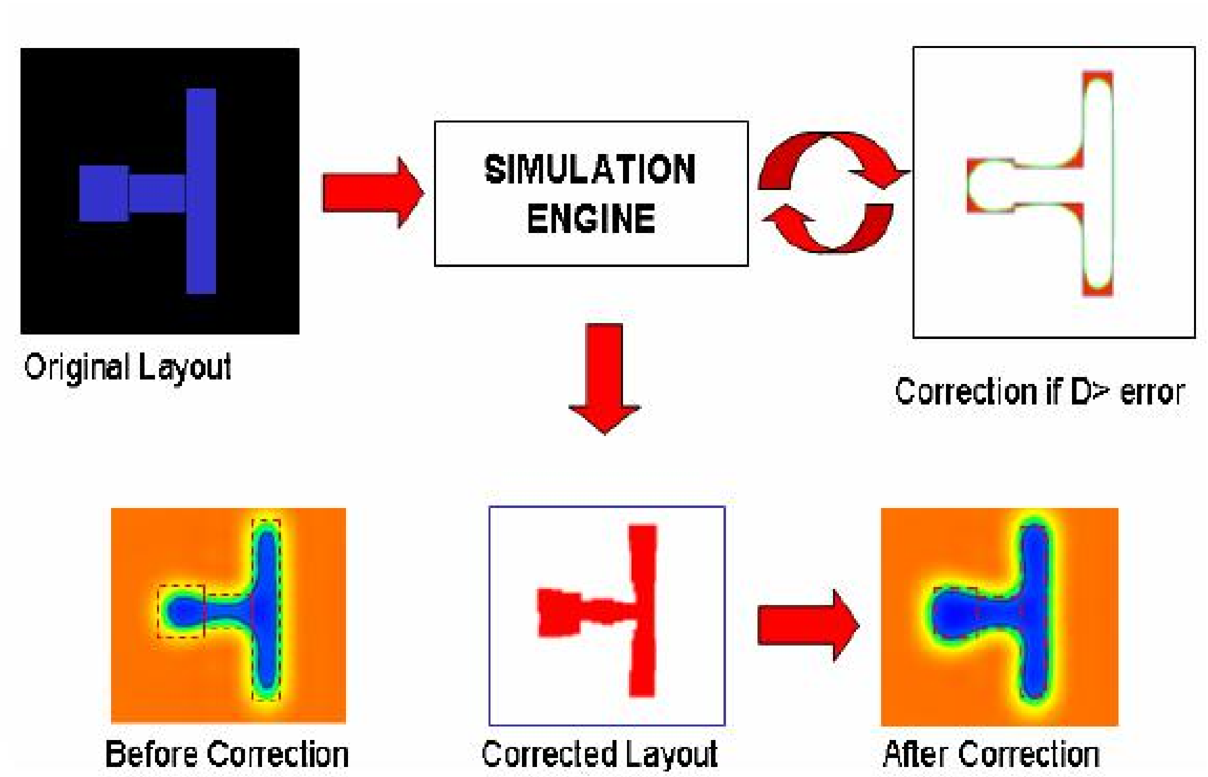


Off axis illumination



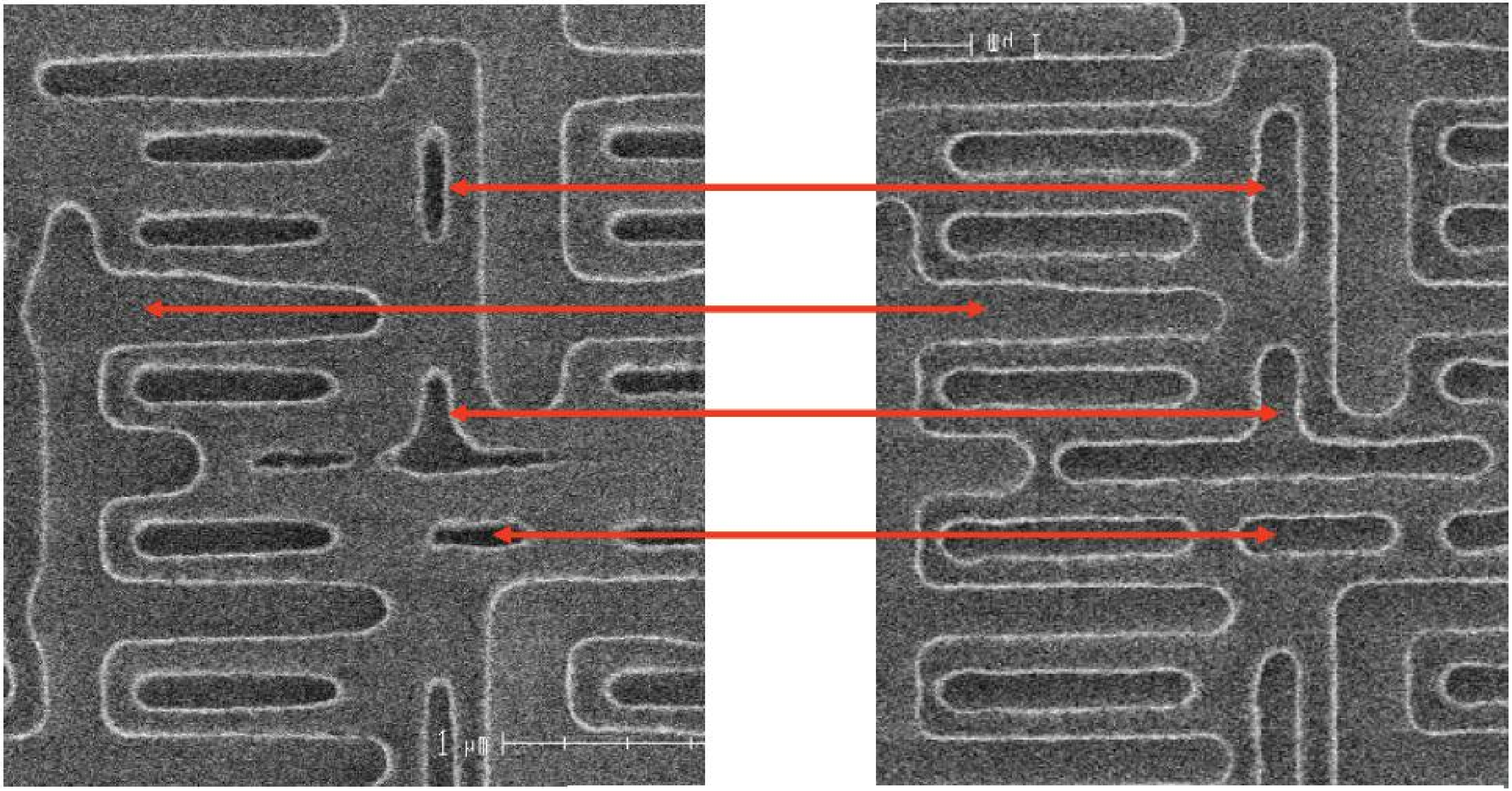
This works well with regular gratings

Optical Proximity Corrections



Needs heavy computer programs to calculate diffraction effects and correct them

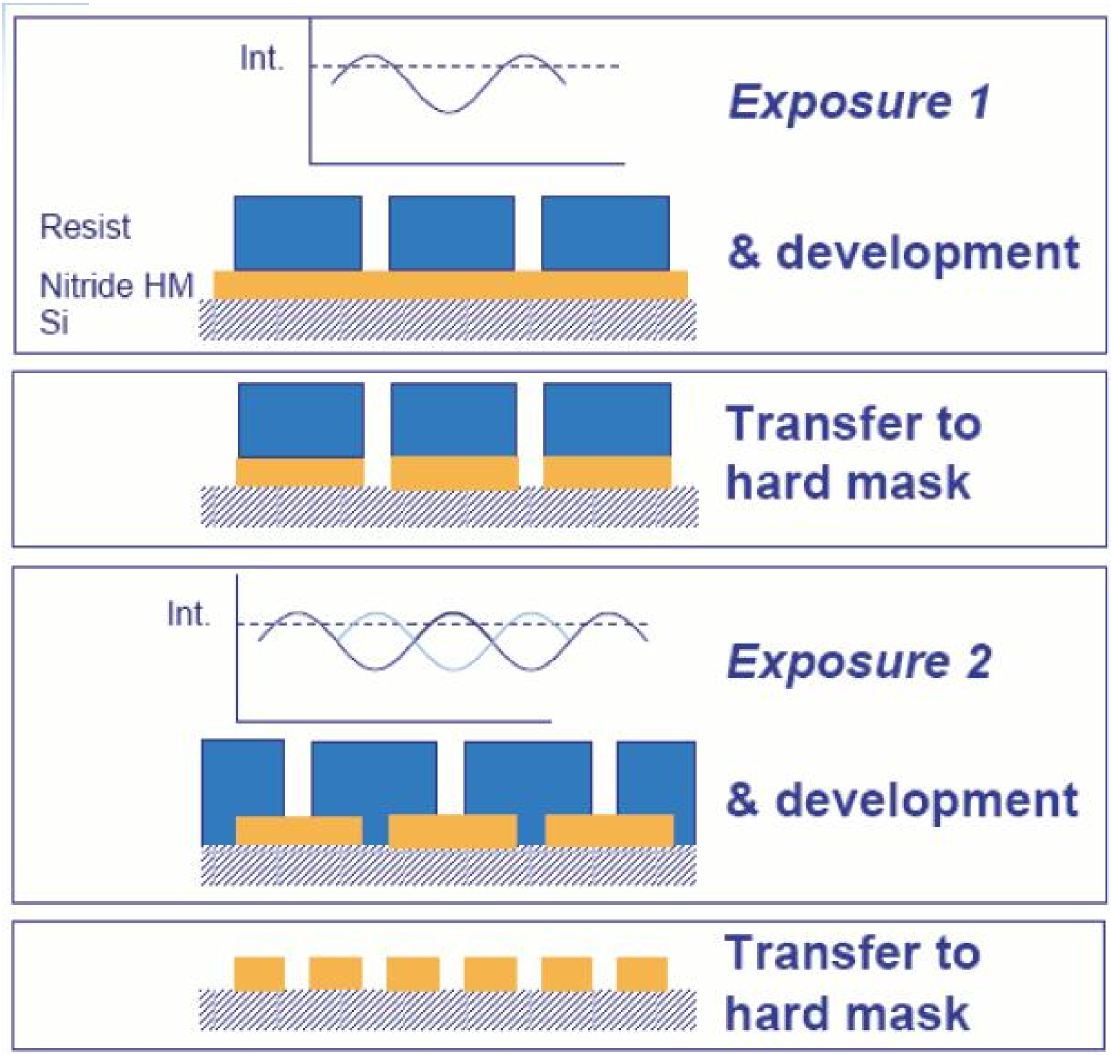
Example



Without mask correction

With mask correction

Double exposure



Exposure 1

& development

Transfer to
hard mask

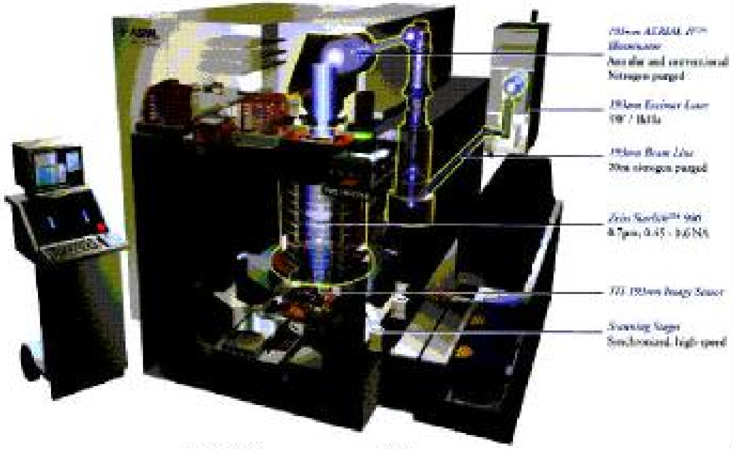
Exposure 2

& development

Transfer to
hard mask

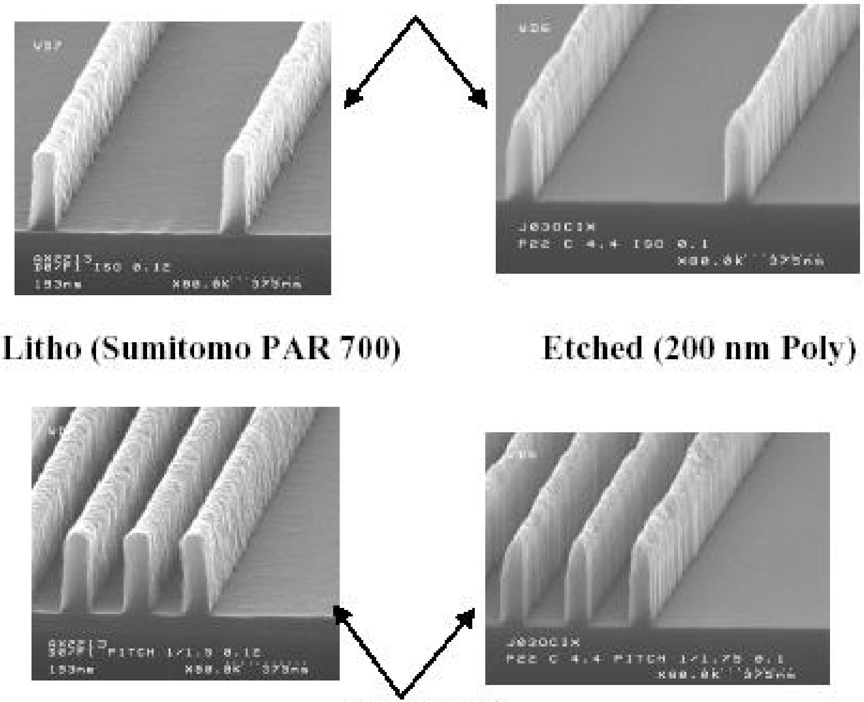
Stepper at 193nm

ASML
PAS5500/900



4X Step and Scan
NA=0.63
Field size 26 mm X 33 mm
Resolution <120 nm
Overlay = 45 nm (mean+3σ)
Throughput > 45 W/H

10M€!



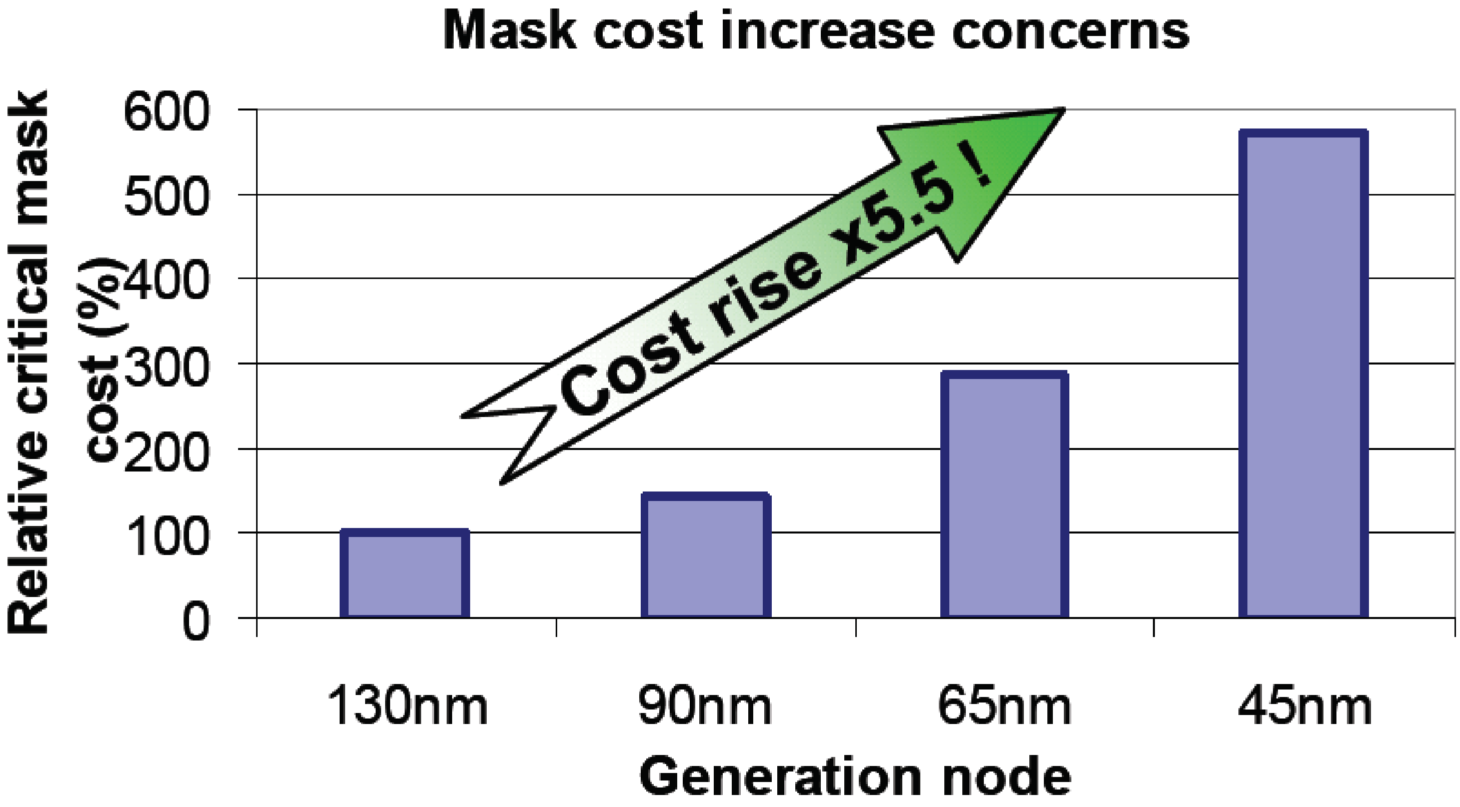
L=100 nm

Litho (Sumitomo PAR 700)

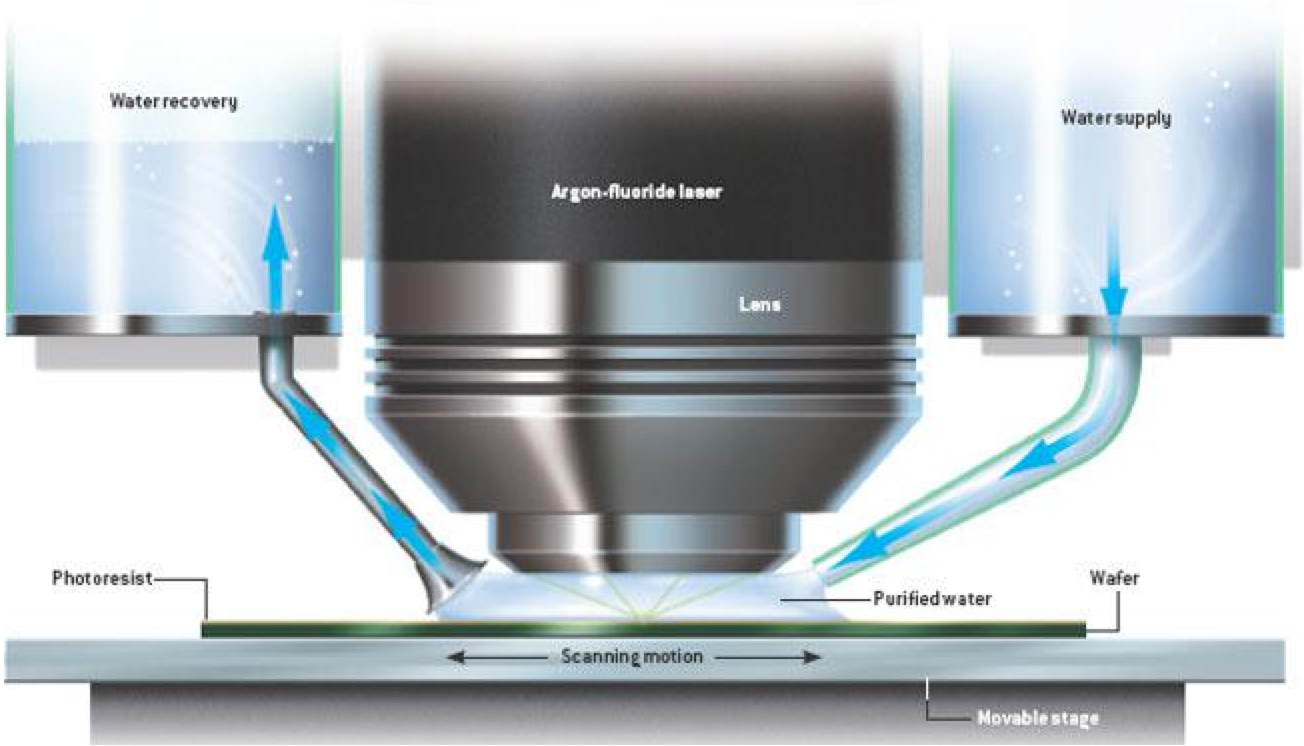
Etched (200 nm Poly)

L=100 nm

S=175 nm


Mask cost increase concerns
Relative critical mask cost (%)
600
500
400
300
200
100
0
Cost rise x5.5 !
130nm
90nm
65nm
45nm
Generation node

Immersion lithography



NA=nsinθ , n of water 1.44 , one can reach NA=1.35

Immersion lithography

Water is very transparent to 193nm

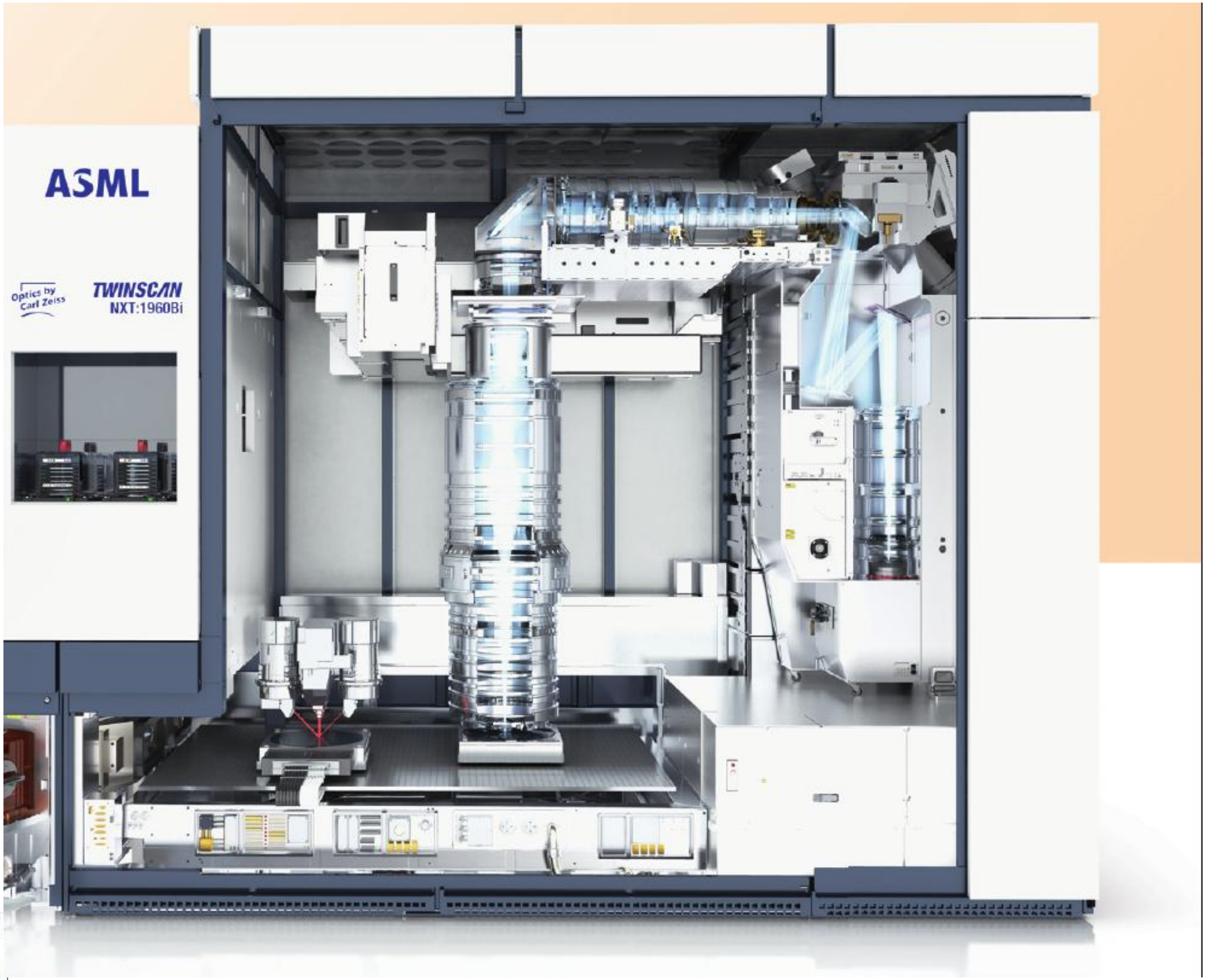
Problems with water:
Water may seem like an easy solution but its implementation presents some serious problems.

Water purification any impurity will introduce absorption
Water/lens interface
Water/resist interactions
Defects
o Backside contamination
o Drying

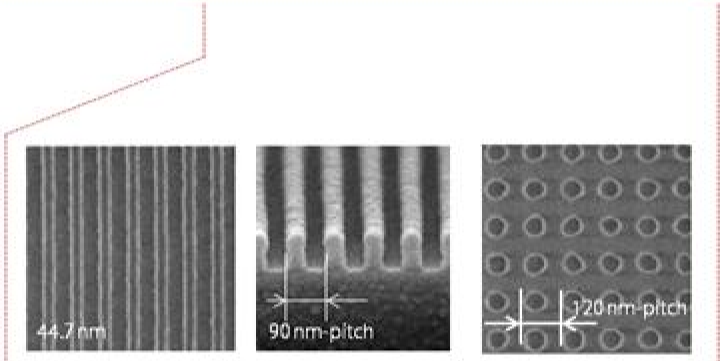
How to keep water contained while in motion (speed of stepper 500cm/s!)

Other complex fluides with higher n are also used

This nowadays a common technique which is in strong competition with EUV



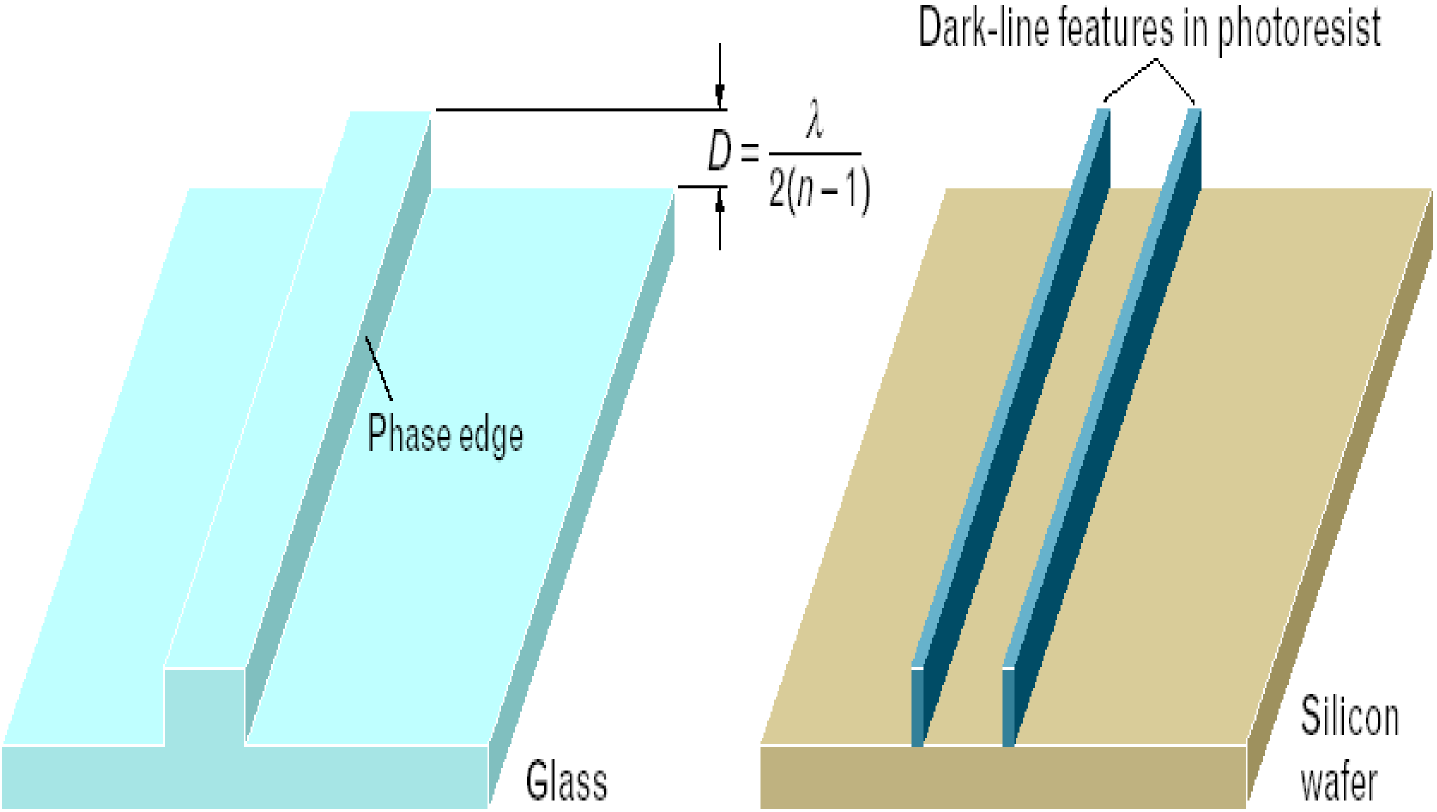
	300 mm line
Front-end (FEOL)	ArF immersion lithography for 45 nm CMOS process
Back-end (BEOL)	Cu wiring using Dual-Damascene



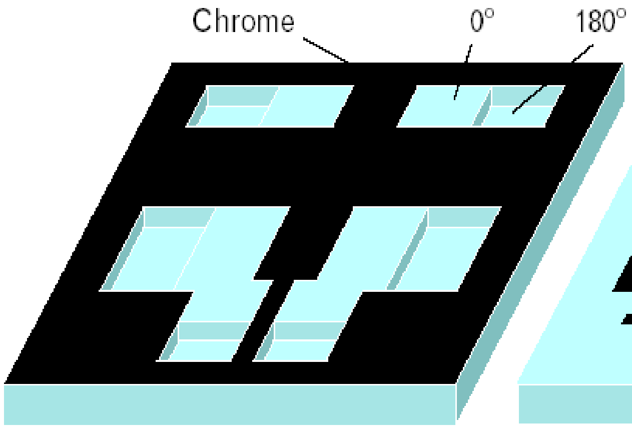
45 nm L & S Pattern

120 nm-pitch/50 nm-CH

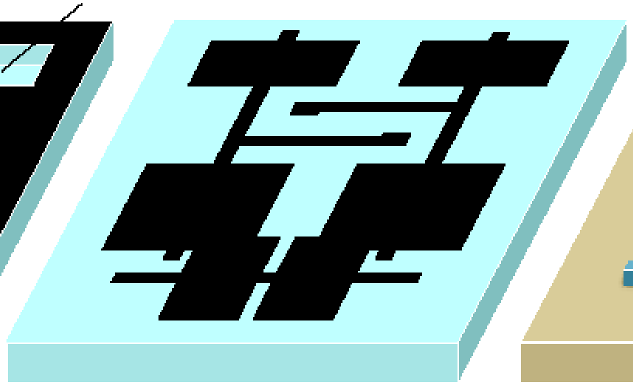
Chromless mask



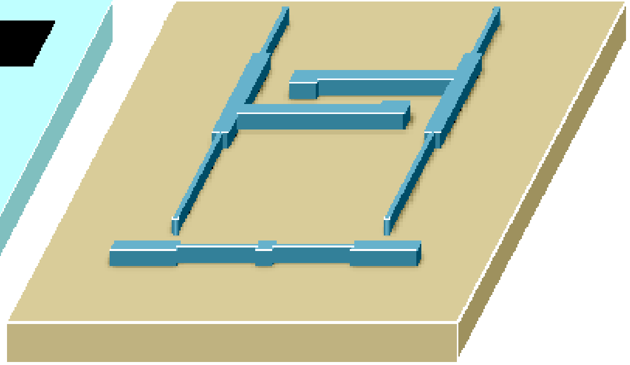
chromeless + double exposure



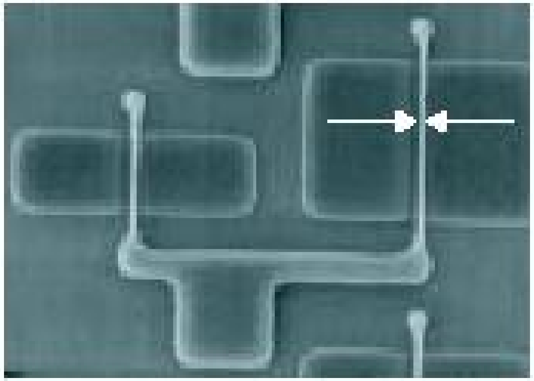
Phase-shift photomask



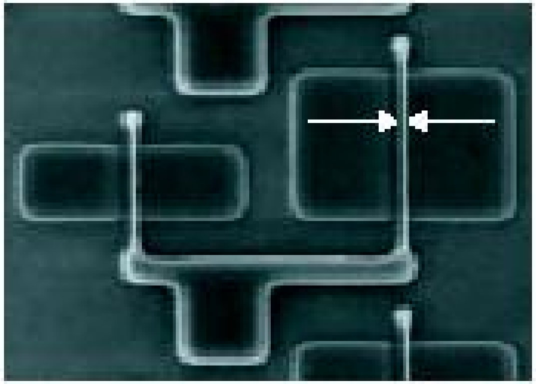
Trim photomask



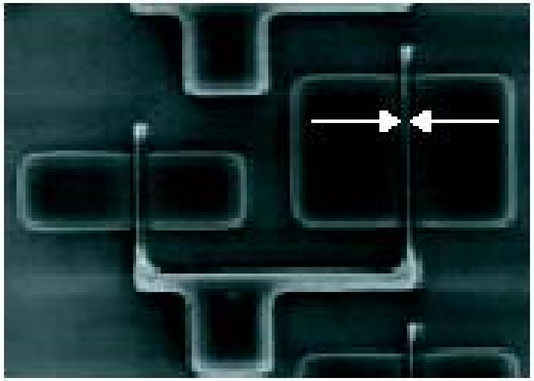
Final pattern on wafer



85-nm gate length



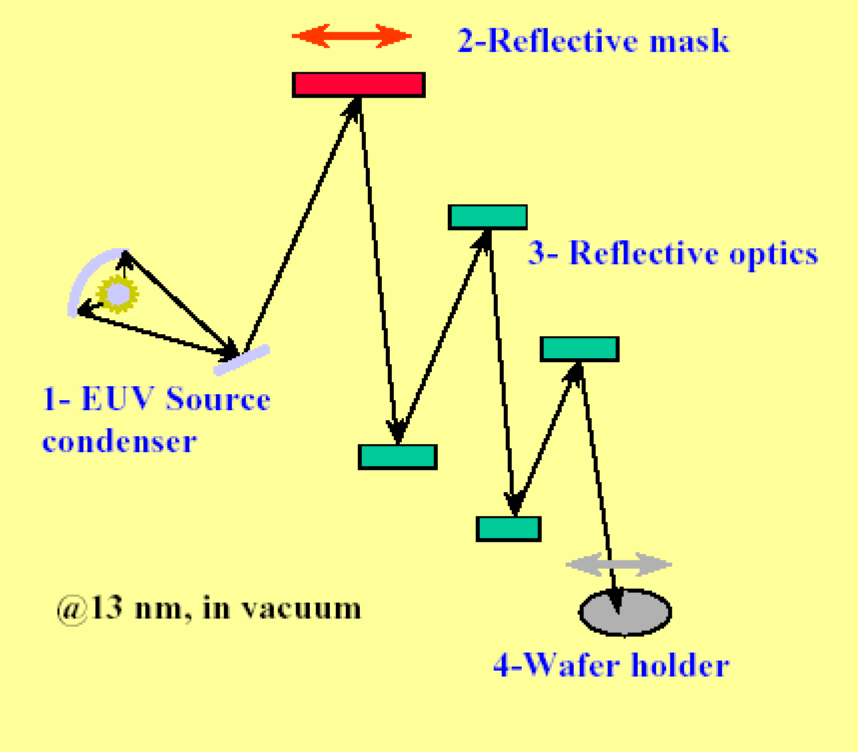
50-nm gate length



25-nm gate length

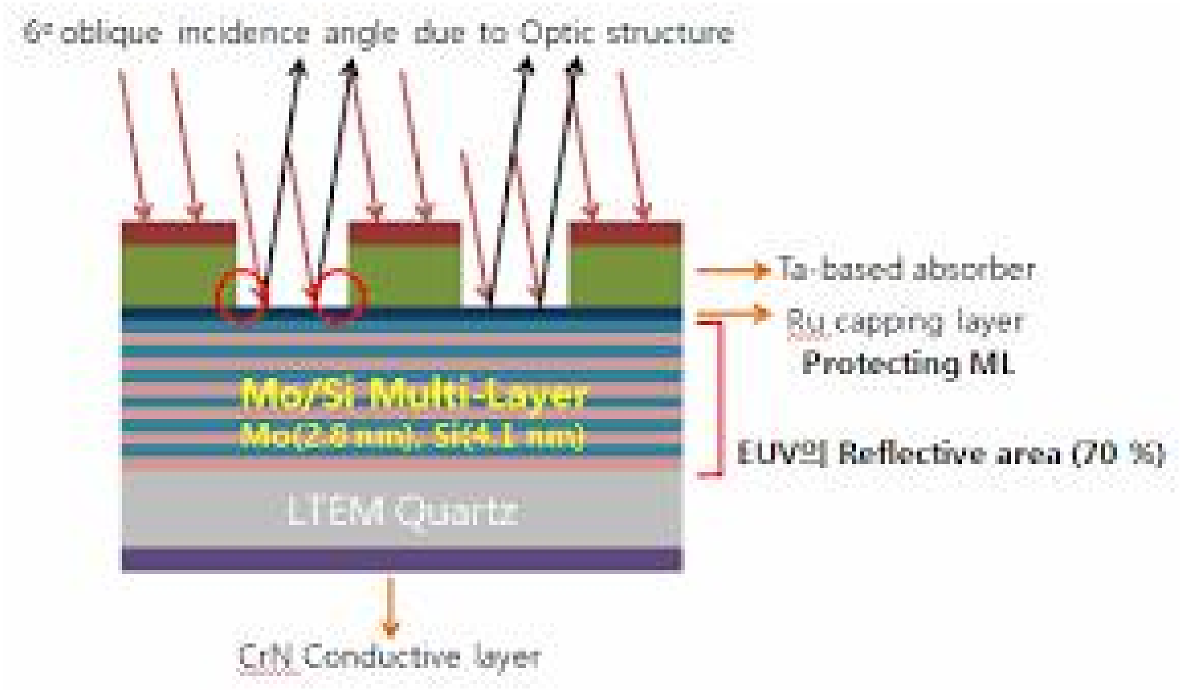
With λ=248nm et NA=0.6 soit un k1=0.06!

EUV Lithography



EUV are rapidely absorb in air
The equipment needs to be in vacuum

EUV reflective mask

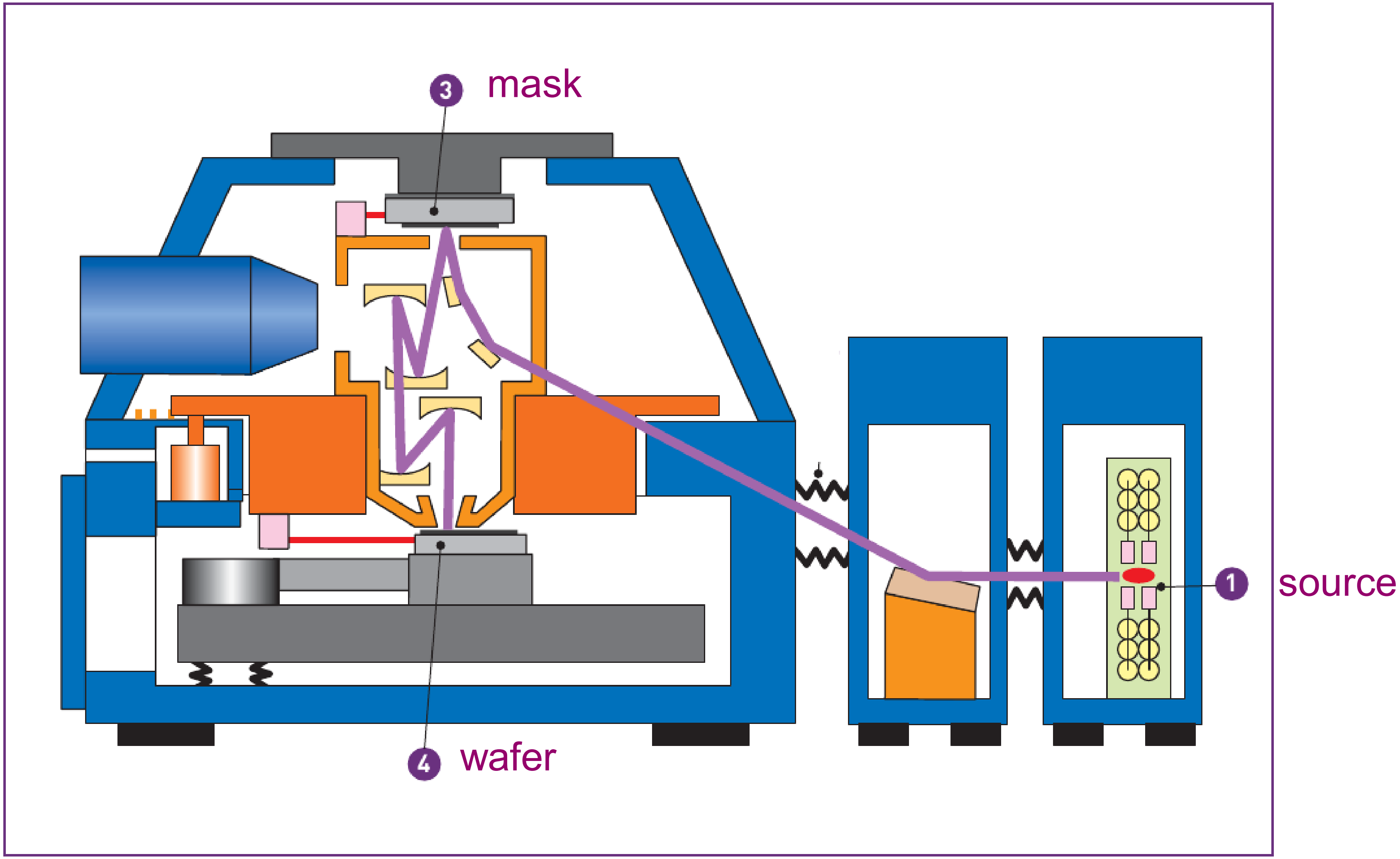


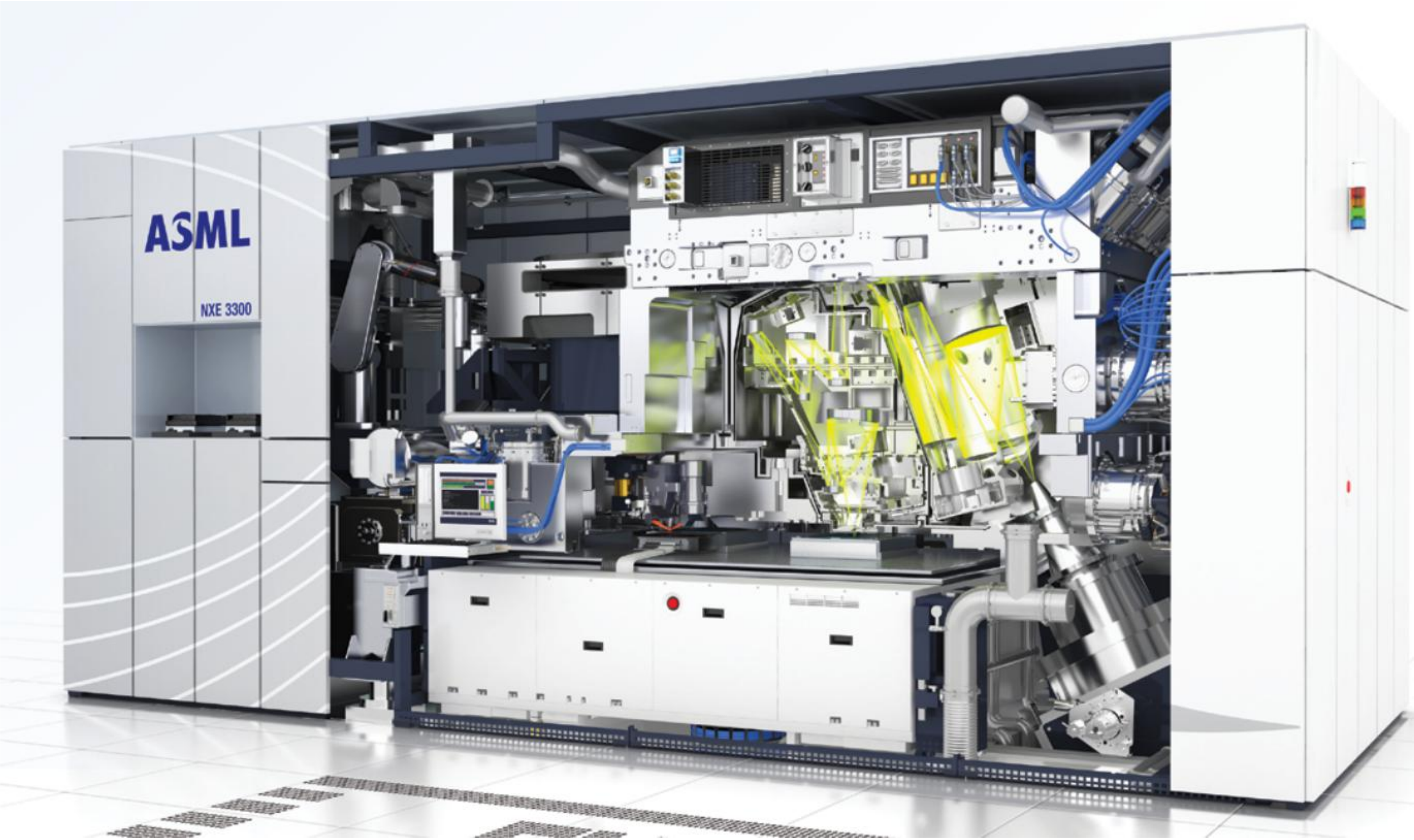
EUV reflective optics : requirements

- Aberrations (For 70 nm CD)
  - -> Surface figure : <0.2nm rms
- Flare (parasitic light => contrast loss))
  - -> Mid spatial frequency roughness : < 0.15nm rms
- Reflectivity loss
  - -> High spatial frequency roughness : < 0.10nm rms

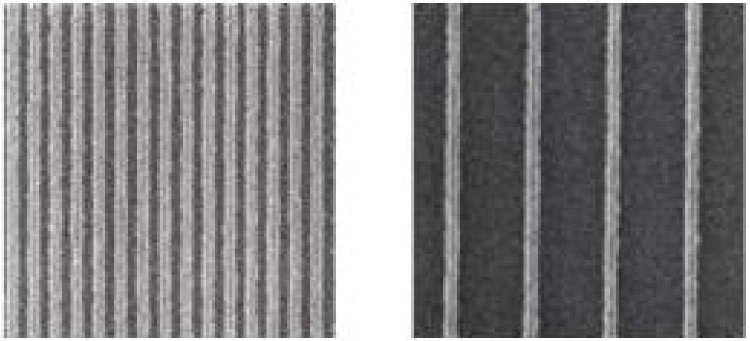
- + Highest possible reflectivity
- + Asphérization
- + Graded multilayer thickness

Big competition between EUV and immersion


③ mask
① source
④ wafer


ASML
NXE 3300

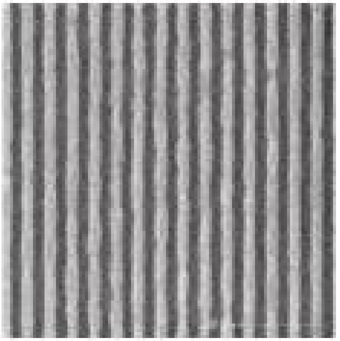
22nm ATP features



Dense lines

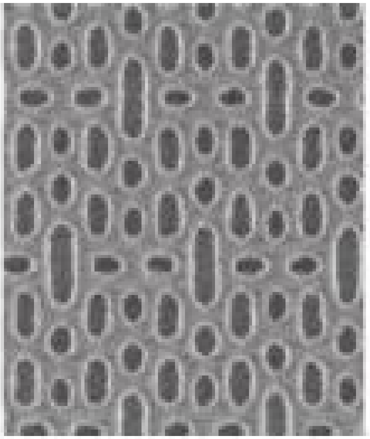
Isolated lines

New Ultimate resolution

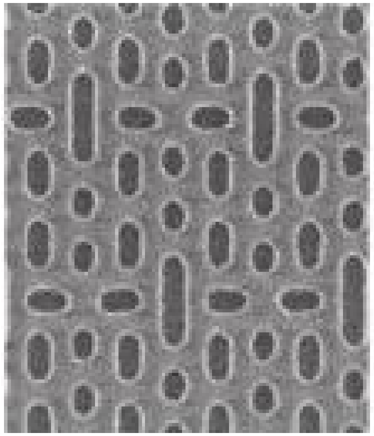


15nm L/S

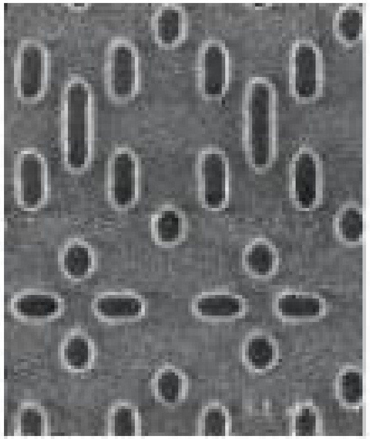
EUV:
14 nm node
Single exposure



EUV:
20 nm node
Single exposure



ArFi:
20 nm node
Double exposure



Costs

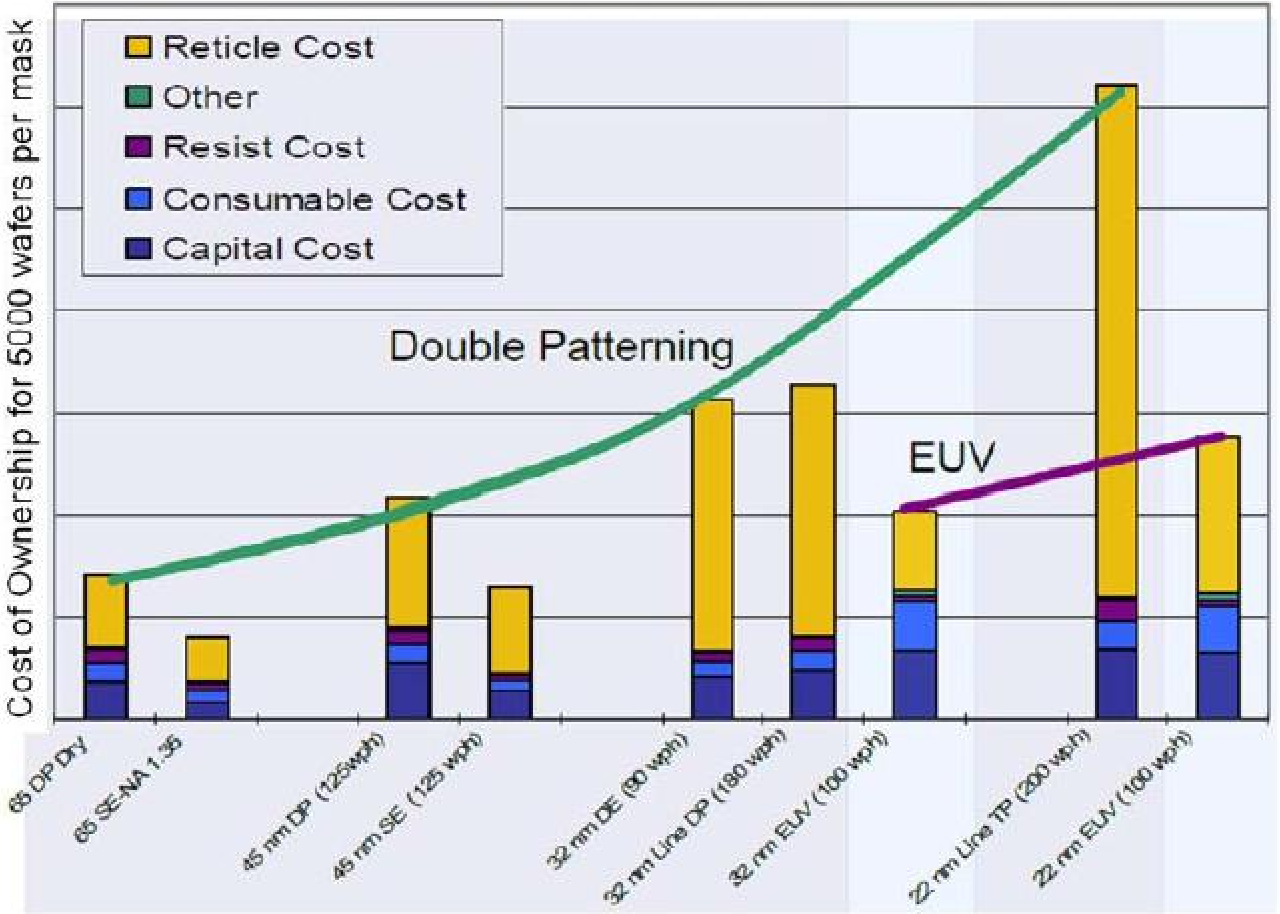


Figure LITH2 Relative Cost of Ownership for the critical level of a 5000 wafer run device

Number of Foundries with a Cutting Edge Logic Fab

SilTerra										
X-FAB										
Dongbu HiTek										
ADI	ADI									
Atmel	Atmel									
Rohm	Rohm									
Sanyo	Sanyo									
Mitsubishi	Mitsubishi									
ON	ON									
Hitachi	Hitachi									
Cypress	Cypress	Cypress								
Sony	Sony	Sony								
Infineon	Infineon	Infineon								
Sharp	Sharp	Sharp								
Freescale	Freescale	Freescale								
Renesas (NEC)	Renesas (NEC)	Renesas (NEC)	Renesas (NEC)	Renesas (NEC)						
SMIC	SMIC	SMIC	SMIC	SMIC						
Toshiba	Toshiba	Toshiba	Toshiba	Toshiba						
Fujitsu	Fujitsu	Fujitsu	Fujitsu	Fujitsu						
TI	TI	TI	TI	TI						
Panasonic	Panasonic	Panasonic	Panasonic	Panasonic	Panasonic					
UMC	UMC	UMC	UMC	UMC	UMC					
STMicroelectronics	STMicroelectronics	STMicroelectronics	STMicroelectronics	STMicroelectronics	STMicroelectronics					
IBM	IBM	IBM	IBM	IBM	IBM	IBM				
AMD	AMD	AMD	GlobalFoundries	GlobalFoundries	GlobalFoundries	GlobalFoundries	GlobalFoundries		GlobalFoundries	
Samsung	Samsung	Samsung	Samsung	Samsung	Samsung	Samsung	Samsung	Samsung	Samsung	
TSMC	TSMC	TSMC	TSMC	TSMC	TSMC	TSMC	TSMC	TSMC	TSMC	
Intel	Intel	Intel	Intel	Intel	Intel	Intel	Intel	Intel	Intel	Future
180 nm	130 nm	90 nm	65 nm	45 nm/40 nm	32 nm/28 nm	22 nm/20 nm	16 nm/14 nm	10 nm	7 nm	5 nm

- 193nm immersion with DE/DP allows to reach 14nm node

- Below 14nm EUVL seems the best candidate

- What about the 7nm node and below ?

People are also thinking to surface plasmon modes or evanescent modes lithography.....